Ref No:

Sri Krishna Institute of Technology,
Bangalore

COURSE PLAN

Academic Year 2019-2020

Program:	B E – Electronics & Communication Engineering
Semester :	6
Course Code:	17EC663
Course Title:	DIGITAL SYSTEM DESIGN USING VERILOG
Credit / L-T-P:	3/3-0-0
Total Contact Hours:	40
Course Plan Author:	ARUN G

Academic Evaluation and Monitoring Cell

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Table of Contents

A. COURSE INFORMATION

1. Course Overview

Degree:	BE	Program:	EC
Semester:	6	Academic Year:	2019-2020
Course Title:	Digital System Design using VERILOG	Course Code:	17EC663
Credit / L-T-P:	3/3-0-0	SEE Duration:	180 Minutes
Total Contact Hours:	40 Hours	SEE Marks:	60
CIA Marks:	40 Marks	Assignment	1 / Module
Course Plan Author:	ARUN G	Sign ..	
Checked By:		Sign ..	
CO Targets	CIA Target :	SEE Target:	

Note: Define CIA and SEE % targets based on previous performance.

2. Course Content

Content / Syllabus of the course as prescribed by University or designed by institute.

Module	Content	Teaching Hours	Blooms Learning Levels
1	Introduction and Methodology: Digital Systems and Embedded Systems, Real-World Circuits, Models, Design Methodology . Combinational Basics: Combinational Components and Circuits, Verification of Combinational Circuits. Sequential Basics: Sequential Datapaths and Control Clocked Synchronous Timing Methodology	08	L1, L2, L3
2	Concepts, Memory Types, Error Detection and Correction	08	L1, L2, L3
3	Implementation Fabrics: Integrated Circuits, Programmable Logic Devices, Packaging and Circuit boards, Interconnection and Signal integrity	08	L1, L2, L3
4	I/O interfacing: I/O devices, I/O controllers, Parallel Buses, Serial Transmission, I/O software	08	L1, L2, L3
5	Design Methodology: Design flow, Design optimization, Design for test, Nontechnical Issues	08	L1, L2, L3,L4
-	**Total**		

3. Course Material

Books & other material as recommended by university (A, B) and additional resources used by course teacher (C).

1. Understanding: Concept simulation / video ; one per concept ; to understand the concepts ; 15 – 30 minutes
2. Design: Simulation and design tools used – software tools used ; Free / open source
3. Research: Recent developments on the concepts – publications in journals; conferences etc.

Modules	Details	Chapters in book	Availability
A	**Text books (Title, Authors, Edition, Publisher, Year.)**	**-**	**-**
1	Peter J. Ashenden, —Digital Design: An Embedded Systems Approach Using VERILOG‖, Elesvier, 2010.	1,2,4,5, 6,8,10	In Lib & Dept
B	**Reference books (Title, Authors, Edition, Publisher, Year.)**	**-**	**-**
1	Samir Palnitkar, —Verilog HDL: A Guide to Digital Design and Synthesis", Pearson Education, Second Edition.		In Lib & Dept

2	Kevin Skahill, —VHDL for Programmable Logic‖, PHI/Pearson education, 2006		In Lib & Dept
3	Donald E. Thomas, Philip R. Moorby, —The Verilog Hardware Description Language‖, Springer Science+Business Media, LLC, Fifth edition.		In Lib & Dept
C	**Concept Videos or Simulation for Understanding**	**-**	**-**
C1	Lab: HDL lab		
C2	Coding and simulation results		
C3	Program FPGAs/CPLDs to synthesize the digital designs		
C4			
C5			
D	**Software Tools for Design**	**-**	**-**
	Familiarize with the CAD tool to write HDL programs.		
E	**Recent Developments for Research**	**-**	**-**
	Synthesize Combinational and Sequential circuits on programmable ICs		
	Interface the hardware to the programmable chips		
F	**Others (Web, Video, Simulation, Notes etc.)**	**-**	**-**
1	https://nptel.ac.in/courses/117101004/		

4. Course Prerequisites

Refer to GL01. If prerequisites are not taught earlier, GAP in curriculum needs to be addressed. Include in Remarks and implement in B.5.
Students must have learnt the following Courses / Topics with described Content . . .

Modules	Course Code	Course Name	Topic / Description	Sem	Remarks	Blooms Level
1	17EC53	Verilog HDL	Hierarchical Modeling Concepts	5		L1,L2
2	17ECL58	HDL lab	Coding and interfacing	5		L1, L2, L3

5. Content for Placement, Profession, HE and GATE

The content is not included in this course, but required to meet industry & profession requirements and help students for Placement, GATE, Higher Education, Entrepreneurship, etc. Identifying Area / Content requires experts consultation in the area.
Topics included are like, a. Advanced Topics, b. Recent Developments, c. Certificate Courses, d. Course Projects, e. New Software Tools, f. GATE Topics, g. NPTEL Videos, h. Swayam videos etc.

Modules	Topic / Description	Area	Remarks	Blooms Level
1	Sequential Datapaths and Control Clocked Synchronous Timing Methodology	VLSI	Recent Developments required to be known for placements and Course projects.	L2
2	Error Detection and Correction	VLSI	Recent Developments required to be known for placements and Course projects.	L2
3	Parallel Buses	VLSI	Recent Developments required to be known for placements and Course projects.	L2
3	Serial Transmission	VLSI	Recent Developments required to be known for placements and Course projects.	L2

B. OBE PARAMETERS

1. Course Outcomes

Expected learning outcomes of the course, which will be mapped to POs.

Modules	Course Code.#	Course Outcome **At the end of the course, student should be able to . . .**	Teach. Hours	Instr Method	Assessment Method	Blooms' Level
1	17EC663.1	Construct the combinational circuits, using discrete gates and programmable logic devices.	2	Chalk , Board & lecture	CIA	L2
2	17EC663.2	Describe Verilog model for sequential circuits and test pattern generation	4	Chalk , Board & lecture	CIA & Assignment	L2
3	17EC663.3	Design a semiconductor memory for specific chip design.	5	Chalk , Board & lecture	CIA	L2
4	17EC663.4	Design embedded systems using small microcontrollers, larger CPUs/DSPs, or hard or soft processor cores	3	Chalk , Board & lecture	CIA	L2
5	17EC663.5	Synthesize different types of processor and I/O controllers that are used in embedded system	4	Chalk , Board & lecture	CIA & Assignment	L2
-	**-**	**Total**		**-**	**-**	**L2-L4**

2. Course Applications

Write 1 or 2 applications per CO.
Students should be able to employ / apply the course learnings to . . .

Modules	Application Area Compiled from Module Applications.	CO	Level
1	Real word circuits, Combinational circuits and circuits, LOW power design	CO1	L2,L3
2	In military applications, Processors design, softcore microcontroller and interfacing	CO2	L2,L3
3	Advanced FPGA Applications, the future of FPGA	CO3	L2
4	FPGA array implementations	CO4	L2
5	The vivado design suite	CO5	L2

3. Articulation Matrix

CO – PO Mapping with mapping level for each CO-PO pair, with course average attainment.

-	-	Course Outcomes	Program Outcomes														-
Modules	CO.#	**At the end of the course student should be able to . . .**	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3	Level
1	CO-1	Construct the combinational circuits, using discrete gates and programmable logic devices	√	√	√										√			L2
2	CO-2	Describe Verilog model for sequential circuits and test pattern generation	√	√		√									√		√	L2
3	CO-3	Design a semiconductor memory for specific chip design.	√		√				√						√			L2
4	CO-4	Design embedded systems using small microcontrollers, larger CPUs/DSPs, or hard or soft processor cores	√	√		√									√			L2
5	CO-5	Synthesize different types of processor and I/O controllers	√	√	√				√						√			L2

		that are used in embedded system																	
-	**17EC663.**	Average																	-
-	*PO, PSO*	*1.Engineering Knowledge; 2.Problem Analysis; 3.Design / Development of Solutions; 4.Conduct Investigations of Complex Problems; 5.Modern Tool Usage; 6.The Engineer and Society; 7.Environment and Sustainability; 8.Ethics; 9.Individual and Teamwork; 10.Communication; 11.Project Management and Finance; 12.Life-long Learning; S1.Software Engineering; S2.Data Base Management; S3.Web Design*																	

4. Curricular Gap and Content

Topics & contents not covered (from A.4), but essential for the course to address POs and PSOs.

Modules	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1		Seminar	2nd week / date	Dr XYZ, Inst	List from B4 above
2		Seminar	3rd Week		

C. COURSE ASSESSMENT

1. Course Coverage

Assessment of learning outcomes for Internal and end semester evaluation.

Modules	Title	Teach. Hours	No. of question in Exam						CO	Levels
			CIA-1	CIA-2	CIA-3	Asg	Extra Asg	SEE		
1	Introduction and methodology	10	2			1	1	2	CO1,CO2	L2
2	Memories	10	2			1	1	2	CO1,CO2	L2
3	Implementation Fabrics	10		2		1	1	2	CO3,CO4	L2
4	I/O interfacing	10		2	2	1		2	CO3,CO4	L2
5	Design Methodology	10			2	1	1	2	CO4,CO5	L2
-	**Total**	**50**	**4**	**4**	**4**	**5**	**5**	**10**	**-**	**-**

2. Continuous Internal Assessment (CIA)

Assessment of learning outcomes for Internal exams. Blooms Level in last column shall match with A.2.

Modules	Evaluation	Weightage in Marks	CO	Levels
1, 2	CIA Exam – 1	30	CO1,CO2	L2
3, 4	CIA Exam – 2	30	CO3,CO4	L2
5	CIA Exam – 3	30	CO4,CO5	L2
1, 2	Assignment - 1	10	CO1,CO2	L2,L2
3, 4	Assignment - 2	10	CO3,CO4	L2,L2
5	Assignment - 3	10	CO4,CO5	L2,L2
1, 2	Seminar - 1		-	-
3, 4	Seminar - 2		-	-
5	Seminar - 3		-	-
1, 2	Quiz - 1		-	-
3, 4	Quiz - 2		-	-
5	Quiz - 3		-	-
1 - 5	Other Activities – Mini Project	-		
	Final CIA Marks	**40**	**-**	**-**

D1. TEACHING PLAN - 1

Module - 1

Title:	Introduction and Methodology	Appr Time:	8 Hrs
a	***Course Outcomes***	**CO**	**Blooms**
	Construct the combinational circuits, using discrete gates and programmable logic devices.	CO1	**L2**
	Describe Verilog model for sequential circuits and test pattern generation.	CO2	L2
	Design a semiconductor memory for specific chip design.	CO1	L2
b	***Course Schedule***	-	-
Class No	**Portion covered per hour**	**-**	**-**
1	Digital Systems and Embedded Systems	CO1	L2
2	Real-World Circuits	CO1	L2
3	Models ,Design Methodology	CO1	L3
4	Combinational Components and Circuits	CO1	L2
5	Verification of Combinational Circuits	CO1	L2
6	Sequential Datapaths	CO1	L2
7	Control Clocked Synchronous Timing Methodology	CO2	L2
8	Design problems	CO2	L2
c	**Application Areas**		
-	Students should be able employ / apply the Module learnings to . . .		
1	Real word circuits, Combinational circuits and circuits	CO1	L2
2	LOW power design	CO2	L2
d	**Review Questions**		
-			
1	Define the term setup time, hold time	CO1	L2
2	Explain functional verification and formal verification	CO1	L2
3	Develop verilog module for 4:1 mux	CO1	L2
4	Explain noise margin and propogation delay	CO1	L2
5	Explain 2 sources of power consumption in digital components	CO2	L2
6	Design an encoder for the burglar alarm that has sensors for each 8 zones	CO2	L2
7	What is the 7-segment code corresponding to the BCD code 0011?	CO1	L2
8	what is the purpose of a multiplexer?	CO1	L2
9	How many select input bits are needed for a 6-to-1 multiplexer?	CO1	L3
10	How can we construct a 2-to-1 multiplexer for 5-bit encoded data inputs?	CO1	L3
e	**Experiences**	-	-
1		CO1	L2
2			

Module – 2

Title:		Appr Time:	8 Hrs
a	***Course Outcomes***	**CO**	**Blooms**
-		-	**Level**
	Design embedded systems using small microcontrollers	CO1	L2
	larger CPUs/DSPs, or hard or soft processor cores	CO2	L2
	Design a semiconductor memory for specific chip design.	CO2	L2
b	***Course Schedule***	-	-
Class No	**Portion covered per hour**	**-**	**-**

1	Concepts	CO2	L2
2	Memory types	CO2	L2
3	Asynchronous static RAM	CO2	L2
4	Synchronous Static RAM	CO2	L2
5	Dynamic RAM	CO2	L2
6	Other memory types	CO2	L2
7	Error Detection and Correction	CO2	L2
8	Other examples	CO2	L2
c	**Application Areas**	**-**	**-**
-	Students should be able employ / apply the Module learnings to . . .	-	-
1	Memories application	CO2	L2
2	Error correction and detection	CO2	L3
d	**Review Questions**	-	-
-			
1	What is the effect of a write operation? What is the effect of a read operation?	CO2	L3
2	What is the difference between RAM and ROM?	CO2	L3
3	What is meant by the terms volatile and nonvolatile?	CO2	L2
4	What is the difference between static and dynamic RAM?	CO2	L3
5	What is meant by the access time of a RAM?	CO2	L2
6	Why are asynchronous SRAMs diffi cult to use in high-speed clocked synchronous designs?	CO2	L2
7	What benefit does a multiport memory have over a single-port memory with multiplexed address and data connections?	CO2	L3
8	How does a FIFO facilitate communication of data between clock domains?	CO2	L3
9	What is the distinction between a soft error and a hard error?	CO2	L3
10	What is a common cause of soft errors in DRAMs?	CO2	L3
11	What corrective action can we take when a parity error is detected?	CO2	L2
12	Using a Hamming code, how many check bits are required for single error correction and double-error detection for 4-bit data words?	CO2	L2
e	**Experiences**	-	-
1		CO3	L2
2			

E1. CIA EXAM – 1

a. Model Question Paper - 1

Crs Code:	17EC663	Sem:	6	Marks:	30	Time:	75 minutes
Course:	Digital System Design using Verilog						

-	-	**Note: Answer any 3 questions, each carry equal marks.**	**Marks**	**CO**	**Level**
1	a	What is Digital system? Explain how the Digital circuits are evolved over the times.	8	CO1	L2
	b	Define the terms setup time, hold time and clock-to-output time of a flip-flop and what are the constraints imposed by these parameters on the circuit operations?	7	CO1	L3
2	a	Develop a test bench model for the 3:8 decoder.	5	CO2	L3
	b	With an example show the distinction between a Moore and Mealy finite-state machine and also draw the corresponding state transition diagram	10	CO2	L2

3	a	Explain Bidirectional tristate data connections . Design a 64K× 8-bit composite memory using four 16K × 8-bit components using Bidirectional tristate data connections.	8	CO1	L2
	b	Develop a Verilog model of the FIFO, which can store up to 256 data items of 16 bits each using 256×16 bit dual port SSRAM for the data storage. The FIFO should provide status outputs *empty* and *full* to indicate the empty and full status of FIFO and FIFO will not be read when it is empty nor be written when it is full and that the write and the read port share a common clock.	7	CO2	L2
4	a	Design a circuit that computes the function $y=ci \times x^2$, where x is a binary-coded input value and ci is a coefficient stored in a flow-through SSRAM. x, ci and y are all signed fixed-point values with 8 pre binary-point and 12 post-binary-point bits. The index i is also an input to the circuit, encoded as a 12-bit unsigned integer. Values for x and i arrive at the input during the cycle when a control input, start, is 1. The circuit should minimize area by using single multiplier to multiply ci by x and then by x again.	8	CO2	L3
	b	What is a common cause of soft errors in DRAMs? Compute the 12-bit ECC word corresponding to the 8-bit data word 01100001.	7	CO2	L2

b. Assignment -1

Model Assignment Questions							
Crs Code:	17EC663	Sem:	6	Marks:	5/10	Time:	75 minutes
Course:	Digital System Design using Verilog						

SNo	Assignment Description	Marks	CO	Level
1	What is meant by the term *design methodology*?		CO1	L3
2	Why is a design methodology beneficial?	5	CO1	L3
3	If verification fails during some stage of a design methodology, what action is taken?		CO1	L2
4	What is meant by *top-down design*?	5	CO1	L3
5	Name two implementation fabrics for digital circuits.	5	CO1	L2
6	What is an embedded system?	5	CO1	L5
7	What is meant by the term *hardware/software codesign*?	5	CO1	L2
8	How does a priority encoder solve the problem of multiple inputs being 1 at the same time?	5	CO1	L2
9	What decimal digit is represented by the BCD code 0101?	5	CO1	L2
10	What is the 7-segment code corresponding to the BCD code 0011?	5	CO1	L2
11	at is the purpose of a multiplexer?	5	CO1	L2
12	How many select input bits are needed for a 6-to-1 multiplexer?	5	CO2	L3
13	How can we construct a 2-to-1 multiplexer for 5-bit encoded data inputs?	5	CO2	L3
14	What logic level would you expect on a signal labeled door_closed, connected to a door sensor, when the door is open?	5	CO2	L3
15	What is the effect of a write operation? What is the effect of a read operation?	5	CO2	L2

16	What is the difference between RAM and ROM?	5	CO2	L3
17	What is meant by the terms volatile and nonvolatile?	5	CO2	L2
18	What is an embedded system?	5	CO2	L2
19	What is meant by the term *hardware/software codesign*?	5	CO2	L2
20	How does a priority encoder solve the problem of multiple inputs being 1 at the same time?	5	CO2	L2

D2. TEACHING PLAN - 2

Module – 3

Title:	Implementation Fabrics	Appr Time:	8 Hrs
a	***Course Outcomes***	**CO**	**Blooms**
-	At the end of the topic the student should be able to . . .	-	**Level**
1	Design a semiconductor memory for specific chip design.	CO3	L2
2	Design embedded systems using small microcontrollers	CO3	L2
b	***Course Schedule***		
Class No	**Portion covered per hour**	**-**	**-**
1	Integrated Circuits	CO3	L2
2	Programmable Logic Devices	CO3	L2
3	Designs on PLA	CO3	L2
4	Packaging	CO3	L2
5	Circuit boards	CO3	L2
6	Interconnection	CO3	L2
7	Signal integrity	CO3	L2
8	Field-Programmable Gate Arrays	CO3	L2
c	**Application Areas**	**-**	**-**
-	Students should be able employ / apply the Module learnings to . . .	-	-
1	Programmable array logic (PAL) components are simple PLDs that implement simple combinational or sequential functions. Generic array logic (GAL) components include programmable macrocells instead of fixed-function output logic.	CO3	L3
2	Signal integrity refers to the minimization of distortion of digital signals due to parasitic capacitance and inductance. Effects include signal skew, ground bounce, transmission line effects (overshoot, undershoot and ringing), electromagnetic interference (EMI), and crosstalk. Effects are mitigated by careful PCB design.	CO3	L3
3	Differential signaling involves transmitting both a positive signal and its negation, and sensing the voltage difference between the two at a receiver. Differential signaling allows common-mode noise rejection and improved signal integrity.	CO3	L3
d	**Review Questions**	-	-
-	The attainment of the module learning assessed through following questions	-	-
1	How does a programmable logic device differ from a fixed-function component?	CO3	L2
2	If crosses were drawn at the intersections (56, 28), (57, 0), (57, 7) and (58, 30) of the diagram in Figure 6.9, what logic function would be implemented?	CO3	L2
3	Suppose the OLMC of Figure 6.12 is used for a state bit S2 of a finite-state machine. For each multiplexer, which input would be selected to make S2 available as an output and to feed it back for use in computing the next-state function?	CO3	L2
4	What other blocks are included in an FPGA?	CO3	L2
5	If an FPGA uses volatile SRAM cells to store configuration information, how is the	CO3	L2

	configuration		
6	What distinguishes a platform FPGA from a simple FPGA?	CO3	L2
7	How does flip-chip IC packaging differ from previous packaging technologies?	CO3	L2
8	What distinguishes surface-mount IC packages from insertion-type packages?	CO3	L2
9	What is meant by the term *signal integrity*?	CO3	L2
10	How fast does a signal change propagate along a typical PCB trace?	CO3	L2
11	What causes ground bounce in digital systems?	CO3	L2
12	Where should bypass capacitors be placed on a PCB?	CO3	L2
13	How does limiting the slew rate of an output driver improve signal integrity?	CO3	L2
15	What design techniques can be used to mitigate transmission-line effects, such as overshoot, undershoot and ringing?	CO3	L2
16	What are *EMI* and *crosstalk*?	CO3	L2
e	**Experiences**	-	-
1		CO6	L2
2			

Module – 4

Title:	I/O Interfacing	Appr Time:	8 Hrs
a	***Course Outcomes***	**CO**	**Blooms**
-	At the end of the topic the student should be able to . . .	-	**Level**
1	Design embedded systems using small microcontrollers	CO4	L2,L3
2	larger CPUs/DSPs	CO4	L2,L3
3	hard or soft processor cores	CO4	L2,L3
b	***Course Schedule***		
Class No	**Portion covered per hour**	**-**	**-**
1	I/O devices	CO4	L2,L3
2	I/O controllers	CO4	L2,L3
3	Parallel Buses	CO4	L2,L3
4	Serial Transmission	CO4	L2,L3
5	I/O software	CO4	L2,L3
6	Multiplexed Buses, Tristate Buses	CO4	L2,L3
7	Polling,Interupts,Timers	CO4	L2,L3
8	Application Areas	CO4	L2,L3
c	**Application Areas**	**-**	**-**
-	Students should be able employ / apply the Module learnings to . . .	-	-
1	Differential signaling involves transmitting both a positive signal and its negation, and sensing the voltage difference between the two at a receiver.	CO4	L3
2	Differential signaling allows common-mode noise rejection and improved signal integrity.	CO4	L3
d	**Review Questions**	-	-
-	The attainment of the module learning assessed through following questions	-	-
1	What is a sensor? What is an actuator?	CO4	L3
2	Why would a digital system require a digital-to-analog converter?	CO4	L3
3	How many comparators are required in a fl ash ADC with a resolution of 8 bits?	CO4	L3
4	How can we reduce the number of connections required for a multi digit 7-segment LED display?	CO4	L3
5	What is the difference between a solenoid and a relay?	CO4	L3
6	Identify two kinds of motor that we might control with a digital system.	CO4	L3

7	If an application requires a 12-bit digital-to-analog converter (DAC), would we choose an R-string DAC or an R/2R ladder DAC? Why?	CO4	L3
8	What is the purpose of an input register in an I/O controller? What is the purpose of an output register?	CO4	L3
9	What is the purpose of a control register in an I/O controller? What is the purpose of a status register?	CO4	L3
10	If an embedded processor uses memory mapped I/O, how do we distinguish accesses to memory from accesses to I/O registers?	CO4	L3
11	Why might a controller for an input device have registers to which a processor can write?	CO4	L3
12	What advantages do autonomous I/O controllers have over simple controllers?	CO4	L2
13	In a multiplexed bus system, why might it be desirable to subdivide the multiplexers and distribute them around the chip?	CO4	L3
14	How does a tristate bus avoid logic-level contention on bus signals?	CO4	L2
15	Why should we avoid floating bus signals?	CO4	L3
16	What problems can arise if we disable one tristate bus driver at the same time	CO4	L3
17	Write a Verilog assignment that represents a tri-state bus driver for an 8-bit bus.	CO4	L3
18	What value results on a Verilog wire net when two tristate drivers are enabled and driving opposite logic levels?	CO4	L3
19	Why is a signal connecting several open-drain drivers called a wired- AND connection?	CO4	L2
20	Write a Verilog declaration that represents an open-drain bus.	CO4	L3
e	**Experiences**	-	-
1		CO4	L2
2			

E2. CIA EXAM – 2

a. Model Question Paper - 2

Crs Code:	17EC663	Sem:	6	Marks:	30	Time:	75 minutes
Course:	Digital System Design using Verilog						

-	-	**Note: Answer all questions, each carry equal marks. Module : 3, 4**	**Marks**	**CO**	**Level**
-	-	**Note: Answer any 2 questions, each carry equal marks.**	**Marks**	**CO**	**Level**
1	a	Explain different types of PCB design. How fast does a signal change propagate along a typical PCB trace?	8	CO4	L2
	b	Explain the concept differential signaling .How does differential signaling improve noise immunity?	7	CO4	L3
2	a	Explain signal integrity interconnection issue in PCB design.	8	CO4	L2
	b	What is the benefit of allowing a PLD in a system to be reprogrammed?	7	CO4	L3
3	a	Explain Digital-to-Analog Converters using R/2R ladder DAC.	8	CO4	L2
	b	Write a Verilog assignment that represents a tri-state bus driver for an 8-bit bus.	7	CO4	L3
4	a	Explain any four serial interface standards.	8	CO4	L2
	b	Design and develop the Verilog code for an input controller that has 8-bit binary-coded input from a sensor. The value can be read from an 8-bit input register. The controller should interrupt the embedded Gumnut core when the input value changes. The controller is the only interrupt source in the system.	7	CO4	L3

b. Assignment – 2

Model Assignment Questions							
Crs Code:	17EC663	Sem:	6	Marks:	5 / 10	Time:	90-120minutes
Course:	Digital System Design Using Verilog						

SNo	Assignment Description	Marks	CO	Level
1	How does a programmable logic device differ from a fixed-function component?	5	CO4	L2
2	If crosses were drawn at the intersections (56, 28), (57, 0), (57, 7) and (58, 30) of the diagram in Figure 6.9, what logic function would be implemented?	5	CO4	L3
3	Suppose the OLMC of Figure 6.12 is used for a state bit S2 of a finite-state machine. For each multiplexer, which input would be selected to make S2 available as an output and to feed it back for use in computing the next-state function?		CO4	L2
4	What other blocks are included in an FPGA?	5	CO4	L3
5	If an FPGA uses volatile SRAM cells to store configuration information, how is the configuration	5	CO4	L2
6	What distinguishes a platform FPGA from a simple FPGA?	5	CO4	L3
7	How does flip-chip IC packaging differ from previous packaging technologies?	5	CO4	L2
8	What distinguishes surface-mount IC packages from insertion-type packages?	5	CO4	L3
9	What is meant by the term *signal integrity*?	5	CO4	L2
10	How fast does a signal change propagate along a typical PCB trace?	5	CO4	L3
11	What causes ground bounce in digital systems?	5	CO4	L2
12	Where should bypass capacitors be placed on a PCB?	5	CO4	L3
13	How does limiting the slew rate of an output driver improve signal integrity?	5	CO4	L2
14	What design techniques can be used to mitigate transmission-line effects, such as overshoot, undershoot and ringing?	5	CO4	L3
15	What are *EMI* and *crosstalk*?	5	CO4	L2
16	How does differential signaling improve noise immunity?	5	CO4	L3
17	For a 2.5V low-voltage differential signaling (LVDS) output, the nominal VOL and VOH voltages are 1.075V and 1.425V, respectively. What differential voltage swing is seen at the receiver?	5	CO4	L2
18	What is a sensor? What is an actuator?	5	CO4	L2
19	Why would a digital system require a digital-to-analog converter?	5	CO4	L3
20	How many comparators are required in a fl ash ADC with a resolution of 8 bits?	5	CO4	L2

D3. TEACHING PLAN - 3

Module – 5

Title:	Design Methodology	Appr Time:	08 Hrs
a	***Course Outcomes***	**CO**	**Blooms**
-	At the end of the topic the student should be able to . . .	-	**Level**
1	Synthesize different types of processor and I/O controllers that are used in embedded system	CO5	L3,L4
b	***Course Schedule***	-	-

Class No	Portion covered per hour	-	-
1	Design flow	CO5	L3
2	Design optimization	CO5	L4
3	Design for test	CO5	L3
4	Nontechnical Issues	CO5	L1
5	Architecture ,Verification ,Synthesis,Optimization	CO5	L3
6	Fault modeling, Fault simulation,BIST	CO5	L2
7	Architecture Exploration, Functional Design	CO5	L3
8	Functional Verification,Synthesis,Physical Design	CO5	L4
c	**Application Areas**	**-**	**-**
-	Students should be able employ / apply the Module learnings to . . .	-	-
1	Differential signaling allows common-mode noise rejection and improved signal integrity.	CO5	L3
d	**Review Questions**	-	-
-	The attainment of the module learning assessed through following questions	-	-
1	What is meant by the term architecture exploration?	CO5	L3
2	What is the distinction between logical partitions and physical partitions of a system?	CO5	L4
3	Identify the information described in a high-level specification of a system.	CO5	L3
4	What is a behavioral model of a component? What is its purpose?	CO5	L1
5	What are the benefits of reusing an IP block to implement a component?	CO5	L3
6	Identify three kinds of function that can be implemented using a core generator.	CO5	L4
7	If several designers are collaborating on development of model code, what tool can they use to coordinate their changes?	CO5	L3
8	What aspects of the design fl ow does a verification plan cover?	CO5	L1
9	Describe the difference between code coverage and functional coverage. Which is more important for ensuring correctness of a design?	CO5	L3
10	Briefly outline how constrained random testing works.	CO5	L4
11	Identify some advantages and disadvantages of formal verification over simulation-based testing.	CO5	L3
12	What is a hardware abstraction layer for embedded software?	CO5	L4
13	Why do RTL synthesis tools only accept a subset of a hardware description language's features?	CO5	L3
14	Why should we perform gate-level simulation of the circuit produced by a synthesis tool?	CO5	L1
15	Briefly describe the purpose of floor planning, placement, and routing.	CO5	L3
16	If we need to achieve a major improvement in system performance, should we focus effort in earlier or later stages of the design fl ow?	CO5	L4
17	How can we affect circuit area during the functional design stage of the design fl ow?	CO5	L2
18	Identify a means of improving system performance that we might consider in the architecture exploration stage. What trade-offs arise from improving performance?	CO5	L1
19	How does a timing budget help a design team to meet timing constraints?	CO5	L3
20	What is the purpose of specifying timing constraints for synthesis?	CO5	L4
21	How does a static timing analyzer verify timing for a synthesized design and for a placed and routed design?	CO5	L2
22	Briefly describe two techniques for reducing power consumption.	CO5	L1
23	Why should clock gating not be implemented in RTL model code? How is it better implemented?	CO5	L3
24	What is meant by the term design for test?	CO5	L4
25	Describe the stuck-at fault model, and identify circuit defects that are	CO5	L2

	represented by the model.		
e	**Experiences**	-	-
1		CO5	L2
2		CO5	

E3. CIA EXAM – 3

a. Model Question Paper - 3

Crs Code:	17EC663	Sem:	6	Marks:	30	Time:	75 minutes
Course:	Digital System Design Using Verilog						

-	-	**Note: Answer any 2 questions, each carry equal marks.**	**Marks**	**CO**	**Level**
1	a	Explain the design flow of Software co-design.	10	CO5	L1
	b	Describe the stuck-at fault model, and identify circuit defects that are represented by the model.	5	CO5	L3
2	a	What purposes do LFSRs and MISRs have in signature-based BIST?	10	CO5	L4
	b	Identify three kinds of function that can be implemented using a core generator.	5	CO5	L2
3	a	Explain the design flow of hardware co-design.	10	CO5	L1
	b	What aspects of the design flow does a verification plan cover?	5	CO5	L3
4	a	**OR**		CO5	L4
	b	Explain Built-in self test (BIST) techniques.	10	CO5	L2
		Explain the terms scan design and boundary scan	5	CO5	L1

b. Assignment – 3

Model Assignment Questions							
Crs Code:	17EC663	Sem:	6	Marks:	5	Time:	75 minutes
Course:	Digital System Design Using Verilog						

SNo	**Assignment Description**	**Marks**	**CO**	**Level**
1	What is meant by the term architecture exploration?	5	CO5	L2
2	What is the distinction between logical partitions and physical partitions of a system?	5	CO5	L3
3	Identify the information described in a high-level specification of a system.	5	CO5	L2
4	What is a behavioral model of a component? What is its purpose?	5	CO5	L3
5	What are the benefits of reusing an IP block to implement a component?	5	CO5	L2
6	Identify three kinds of function that can be implemented using a core generator.	5	CO5	L4
7	If several designers are collaborating on development of model code ,what tool can they use to coordinate their changes?	5	CO5	L3
8	What aspects of the design fl ow does a verifi cation plan cover?	5	CO5	L3
9	Describe the difference between code coverage and functional coverage. Which is more important for ensuring correctness of a design?	5	CO5	L3
10	Briefly outline how constrained random testing works.	5	CO5	L3
11	Identify some advantages and disadvantages of formal verification over simulation-based testing.	5	CO5	L3
12	What is a hardware abstraction layer for embedded software?	5	CO5	L3
13	Why do RTL synthesis tools only accept a subset of a hardware	5	CO5	L2

	description language's features?			
14	Why should we perform gate-level simulation of the circuit produced by a synthesis tool?	5	CO5	L3
15	Briefl y describe the purpose of floor planning, placement, and routing.	5	CO5	L3
16	If we need to achieve a major improvement in system performance,should we focus effort in earlier or later stages of the design fl ow?	5	CO5	L3
17	What is meant by a circuit node being controllable and observable?	5	CO5	L3
18	Identify an advantage and a disadvantage of scan design over testing using external pins only.	5	CO5	L3
19	What circuits are added to a system for built-in self test?	5	CO5	L3
20	Why is BIST useful after manufacturing test of a system?	5	CO5	L3

F. EXAM PREPARATION

1. University Model Question Paper

Course:	Digital System Design Using Verilog					Month / Year	May /2019	
Crs Code:	17EC663	Sem:	6	Marks:	100	Time:	180 minutes	
Module		Answer all FIVE full questions. All questions carry equal marks.				**Marks**	**CO**	**Level**
1	a	What is Digital system? Explain how the Digital circuits are evolved over the times.				5	CO1	L3
	b	Define the terms setup time, hold time and clock-to-output time of a flip-flop and what are the constraints imposed by these parameters on the circuit operations?				5	CO1	L3
	c	Develop a Verilog model for a 7-segment decoder. Include an additional input, blank, that overrides the BCD input and causes all segments not to be lit.				6	CO1	L4
		OR						
2	a	Develop a test bench model for the 3:8 decoder.				6	CO1	L2
	b	With an example show the distinction between a Moore and Mealy finite-state machine and also draw the corresponding state transition diagram				10	CO1	L3
3	a	Explain Bidirectional tristate data connections . Design a 64K× 8-bit composite memory using four 16K × 8-bit components using Bidirectional tristate data connections.				8	CO2	L3
	b	Develop a Verilog model of the FIFO, which can store up to 256 data items of 16 bits each using 256×16 bit dual port SSRAM for the data storage. The FIFO should provide status outputs *empty* and *full* to indicate the empty and full status of FIFO and FIFO will not be read when it is empty nor be written when it is full and that the write and the read port share a common clock.				8	CO2	L3
		OR						
4	a	Design a circuit that computes the function $y=ci \times x^2$, where x is a binary-coded input value and ci is a coefficient stored in a flow-through SSRAM. x, ci and y are all signed fixed-point values with 8 pre binary-point and 12 post-binary-point bits. The index i is also an input to the circuit, encoded as a 12-bit unsigned integer. Values for x and i arrive at the input during the cycle when a control input, start, is 1. The circuit should minimize area by using single multiplier to multiply ci by x and then by x again.				8	CO2	L4
	b	What is a common cause of soft errors in DRAMs? Compute the 12-bit ECC word corresponding to the 8-bit data word 01100001.				8	CO2	L3
5	a	Explain different types of PCB design. How fast does a signal change propagate along a typical PCB trace?				8	CO3	L2
	b	Explain the concept differential signaling .How does differential				8	CO3	L2

		signaling improve noise immunity?			
		OR			
6	a	Explain signal integrity interconnection issue in PCB design.	6	CO3	L2
	b	What is the benefit of allowing a PLD in a system to be reprogrammed?	5	CO3	L2
	c	What distinguishes a platform FPGA from a simple FPGA?	5	CO3	L2
7	a	Explain Digital-to-Analog Converters using R/2R ladder DAC.	6	CO4	L2
	b	Write a Verilog assignment that represents a tristate bus driver for an 8-bit bus.	6	CO4	L3
	c	How does the processor determine where to resume program execution on completion of handling an interrupt?	4	CO4	L3
		OR			
8	a	Explain any four serial interface standards.	8	CO4	L2
	b	Design and develop the Verilog code for an input controller that has 8-bit binary-coded input from a sensor. The value can be read from an 8-bit input register. The controller should interrupt the embedded Gumnut core when the input value changes. The controller is the only interrupt source in the system.	8	CO4	L2
9	a	Explain the design flow of hardware/software co-design.	10	CO5	L2
	b	What aspects of the design flow does a verification plan cover?	6	CO5	L2
		OR			
10	a	Explain Built-in self test (BIST) techniques.	8	CO5	L3
	b	Explain the terms scan design and boundary scan	8	CO5	L3

2. SEE Important Questions

Course:	Digital System Design Using Verilog					Month / Year	May 2019	
Crs Code:	17EC663	Sem:	6	Marks:	100	Time:	180 minutes	
	Note	Answer all FIVE full questions. All questions carry equal marks.				-	-	
Module	Qno.	Important Question				**Marks**	**CO**	**Year**
1	1	What is Digital system? Explain how the Digital circuits are evolved over the times.				5	CO1	2018
	2	Define the terms setup time, hold time and clock-to-output time of a flip-flop and what are the constraints imposed by these parameters on the circuit operations?				5	CO1	2018
	3	Develop a Verilog model for a 7-segment decoder. Include an additional input, blank, that overrides the BCD input and causes all segments not to be lit.				6	CO1	2018
	4	Develop a test bench model for the 3:8 decoder.				6	CO1	2018
	5	With an example show the distinction between a Moore and Mealy finite-state machine and also draw the corresponding state transition diagram				10	C01	2018
2	1	Explain Bidirectional tristate data connections . Design a 64K× 8-bit composite memory using four 16K × 8-bit components using Bidirectional tristate data connections.				08	CO2	2018
	2	Develop a Verilog model of the FIFO, which can store up to 256 data items of 16 bits each using 256×16 bit dual port SSRAM for the data storage. The FIFO should provide status outputs *empty* and *full* to indicate the empty and full status of FIFO and FIFO will not be read when it is empty nor be written when it is full and that the write and the read port share a common clock.				08	CO2	2018
	3	Design a circuit that computes the function $y=ci \times x^2$, where x is a binary-coded input value and ci is a coefficient stored in a flow-through SSRAM. x, ci and y are all signed fixed-point values with 8 pre binary-point and 12 post-binary-point bits. The index i is also an				8	CO2	2018

		input to the circuit, encoded as a 12-bit unsigned integer. Values for *x* and *i* arrive at the input during the cycle when a control input, start, is 1. The circuit should minimize area by using single multiplier to multiply *ci* by *x* and then by *x* again.			
	4	What is a common cause of soft errors in DRAMs? Compute the 12-bit ECC word corresponding to the 8-bit data word 01100001.	8	CO2	2018
3	1	Explain different types of PCB design. How fast does a signal change propagate along a typical PCB trace?	8	CO3	2018
	2	Explain the concept differential signaling .How does differential signaling improve noise immunity?	8	CO3	2018
	3	Explain signal integrity interconnection issue in PCB design.	6	CO3	2018
	4	What is the benefit of allowing a PLD in a system to be reprogrammed?	5	CO3	2018
	5	What distinguishes a platform FPGA from a simple FPGA?	5	CO3	2018
4	1	Explain Digital-to-Analog Converters using R/2R ladder DAC.	6	CO4	2018
	2	Write a Verilog assignment that represents a tristate bus driver for an 8-bit bus.	6	CO4	2018
	3	How does the processor determine where to resume program execution on completion of handling an interrupt?	4	CO4	2018
	4	Explain any four serial interface standards.	8	CO4	2018
	5	Design and develop the Verilog code for an input controller that has 8-bit binary-coded input from a sensor. The value can be read from an 8-bit input register. The controller should interrupt the embedded Gumnut core when the input value changes. The controller is the only interrupt source in the system.	8	CO4	2018
5	1	Explain the design flow of hardware/software co-design.	10	CO5	2018
	2	What aspects of the design flow does a verification plan cover?	6	CO5	2018
	3	Explain Built-in self test (BIST) techniques.	8	CO5	2018
	4	Explain the terms scan design and boundary scan	8	CO5	2018

Course Outcome Computation

Academic Year:

Odd / Even semester

INTERNAL TEST	**T1**						**T2**					
Course Outcome	**CO1**		**CO2**		**CO3**		**CO4**		**CO5**		**CO6**	
QUESTION NO	**Q1**	**LV**	**Q2**	**LV**	**Q3**	**LV**	**Q1**	**LV**	**Q2**	**LV**	**Q3**	**LV**
MAX MARKS	10	-	10	-	10	-	10	-	10	-	10	-
USN-1	5	2	10				10	3	9	3	4	1
USN-2	5	2	8	3								
USN-3	7	3	7	3	10	3	8	3	8	3	5	2
USN-4					4	1	10	3	8	3	6	2
USN-5	8	3	6	2	9	3	10	3	8	3		
USN-6							10	3	9	3	4	1
Average CO Attainment		2.5		2.75		2.33		3		3		1.5

LV Threshold : 3:>60%, 2:>=50% and <=60%, 1: <=49%
CO1 Computation :(2+2+2+3)/4 = 10/4=2.5

PO Computation

Program Outcome	PO1		PO3		PO3		PO1		PO12		PO12	
Weight of CO - PO	3		1		3		2		2		3	
Course Outcome	CO1		CO2		CO3		CO4		CO5		CO6	
Test/Quiz/Lab	T1						T2					
QUESTION NO	Q1	LV	Q2	LV	Q3	LV	Q1	LV	Q2	LV	Q3	LV
MAX MARKS	10	-	10	-	10	-	10	-	10	-	10	-
USN-1	5	2	10	3			10	3	9	3	4	1
USN-2	5	2	8	3								
USN-3	7	3	7	3	10	3	8	3	8	3	5	2
USN-4					4	1	10	3	8	3	6	2
USN-5	8	3	6	2	9	3	10	3	8	3		
USN-6							10	3	9	3	4	1
Average CO Attainment		2.5		2.75		2.33		3		3		1.5