Ref No:

Sri Krishna Institute of Technology,
Bangalore

COURSE PLAN

Academic Year 2019-2020

Program:	B E – Electronics & Communication Engineering
Semester :	6
Course Code:	17EC63
Course Title:	VLSI Design
Credit / L-T-P:	4 / 4-0-0
Total Contact Hours:	60
Course Plan Author:	ARUN KUMAR R

Academic Evaluation and Monitoring Cell

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A. COURSE INFORMATION

1. Course Overview

Degree:	BE	Program:	EC
Semester:	6	Academic Year:	2019-20
Course Title:	VLSI Design	Course Code:	17EC63
Credit / L-T-P:	4 / 4-0-0	SEE Duration:	180 Minutes
Total Contact Hours:	50 Hours	SEE Marks:	60 Marks
CIA Marks:	40 Marks	Assignment	1 / Module
Course Plan Author:	ARUN KUMAR R	Sign ..	Dt:
Checked By:		Sign ..	Dt:
CO Targets	CIA Target : 84 %	SEE Target:	55

Note: Define CIA and SEE % targets based on previous performance.

2. Course Content

Content / Syllabus of the course as prescribed by University or designed by institute.

Module	Content	Teaching Hours	Blooms Learning Levels
1	Introduction: A Brief History, MOS Transistors, MOS Transistor Theory, Ideal I-V Characteristics, Non-ideal I-V Effects, DC Transfer Characteristics Fabrication: nMOS Fabrication, CMOS Fabrication[P-well process, N-well process, Twin tub process], BiCMOS Technology	10	L1, L2
2	MOS and BiCMOS Circuit Design Processes: MOS Layers, Stick Diagrams, Design Rules and Layout. Basic Circuit Concepts: Sheet Resistance, Area Capacitances of Layers, Standard Unit of Capacitance, Some Area Capacitance Calculations, Delay Unit, Inverter Delays, Driving Large Capacitive Loads	10	L2,L3
3	Scaling of MOS Circuits: Scaling Models & Scaling Factors for Device Parameters Subsystem Design Processes: Some General considerations, An illustration of Design Processes- Regularity, Design of an ALU Subsystem, The Manchester Carry-chain and Adder Enhancement Techniques	10	L3, L2
4	Subsystem Design: Some Architectural Issues, Switch Logic, Gate(restoring) Logic, Parity Generators, Multiplexers, The Programmable Logic Array (PLA) FPGA Based Systems: Introduction, Basic concepts, Digital design and FPGA's, FPGA based System design, FPGA architecture, Physical design for FPGA's	10	L3, L2
5	Memory, Registers and Aspects of system Timing- System Timing Considerations, Some commonly used Storage/Memory elements Testing and Verification: Introduction, Logic Verification, Logic Verification Principles, Manufacturing Test Principles, Design for testability	10	L3, L2
-	**Total**	**50**	**L2-L3**

3. Course Material

Books & other material as recommended by university (A, B) and additional resources used by course teacher (C).

1. Understanding: Concept simulation / video ; one per concept ; to understand the concepts ; 15 – 30 minutes
2. Design: Simulation and design tools used – software tools used ; Free / open source
3. Research: Recent developments on the concepts – publications in journals; conferences etc.

Modules	Details	Chapters in book	Availability
A	**Text books (Title, Authors, Edition, Publisher, Year.)**	**-**	**-**
1,2,3 4,5	**"Basic VLSI Design"**- Douglas A. Pucknell & Kamran Eshraghian, PHI 3rd Edition (original Edition – 1994).	1,3,4,5,6, 7,8,9	In Lib In dept
1,5	**"CMOS VLSI Design- A Circuits and Systems Perspective"-** Neil H.E. Weste, David Harris, Ayan Banerjee, 3rd Edition, Pearson Education.	1,2,12	In Lib
4	**"FPGA Based System Design"-**Wayne Wolf, Pearson Education, 2004, Technology and Engineering.	1,3,4	In Lib
B	**Reference books (Title, Authors, Edition, Publisher, Year.)**	**-**	**-**
C	**Concept Videos or Simulation for Understanding**	**-**	**-**
C1	Working of MOSFET: https://youtu.be/4_nGFY7zgDM – 16 mins https://www.youtube.com/watch?v=p4E1to95w_w – 48 mins		
C1	Fabrication of MOSFET https://www.youtube.com/watch?v=t-Ve1-oboGo – 14 mins https://www.youtube.com/watch?v=88eYPWShO5c – 58 mins		
C2	Stick diagram and Layout diagrams https://www.youtube.com/watch?v=wqRGa5sOUmc – 10 mins https://www.youtube.com/watch?v=pBS7vBo2zvo – 21 mins		
C2	Sheet resistance and area capacitance calculation https://www.youtube.com/watch?v=iG7X3sYffXU – 10 mins https://www.youtube.com/watch?v=ZqHNUeGbj3U – 8 mins		
C3	Scaling of MOS circuits https://www.youtube.com/watch?v=nAysnNtrbOo – 26 mins https://www.youtube.com/watch?v=S7qcn75NlrA – 12 mins		
C3	Design of full adder, adder enhancement techniques https://www.youtube.com/watch?v=p4jgNRjwluA – 12 mins https://www.youtube.com/watch?v=1lUbwASkPTc – 4 mins	-	-
C4	Switch logic and gate logic https://www.youtube.com/watch?v=EusSZWTjjBE – 12 mins https://www.youtube.com/watch?v=o9vEnzLL-lY – 20 mins		
C4	FPGA based systems https://www.youtube.com/watch?v=L2wsockKwPQ – 4 mins https://www.youtube.com/watch?v=7Zy3kp3pUWI – 1 hr:23 mins		
C5	Memory and registers https://www.youtube.com/watch?v=c3V8w2Wk-D0 – 11 mins https://www.youtube.com/watch?v=fpnE6UAfbtU – 12 mins		
C5	Testing and verification https://www.youtube.com/watch?v=lRf_UPXOnVU – 30 mins https://www.youtube.com/watch?v=-4XBm5t7_Jg – 54 mins		
D	**Software Tools for Design**	**-**	**-**
	Tanner EDA		
	Cadence		
E	**Recent Developments for Research**	**-**	**-**
	https://www.youtube.com/watch?v=TXxw1kdF5_Q		
	https://www.youtube.com/watch?v=Jctk0DI7YP8		
F	**Others (Web, Video, Simulation, Notes etc.)**	**-**	**-**
1	https://www.youtube.com/watch?v=9SnR3M3CIm4		
2	http://nptel.vtu.ac.in/econtent/courses/ECE/06EC56/index.php		

4. Course Prerequisites

Refer to GL01. If prerequisites are not taught earlier, GAP in curriculum needs to be addressed. Include in Remarks and implement in B.5.
Students must have learnt the following Courses / Topics with described Content . . .

Modules	Course Code	Course Name	Topic / Description	Sem	Remarks	Blooms Level
2,3,4	17EC34	Digital Electronics	Design of combinational logic circuits and sequential circuits	3		L2

5. Content for Placement, Profession, HE and GATE

The content is not included in this course, but required to meet industry & profession requirements and help students for Placement, GATE, Higher Education, Entrepreneurship, etc. Identifying Area / Content requires experts consultation in the area.
Topics included are like, a. Advanced Topics, b. Recent Developments, c. Certificate Courses, d. Course Projects, e. New Software Tools, f. GATE Topics, g. NPTEL Videos, h. Swayam videos etc.

Modules	Topic / Description	Area	Remarks	Blooms Level

B. OBE PARAMETERS

1. Course Outcomes

Expected learning outcomes of the course, which will be mapped to POs.

Modules	Course Code.#	Course Outcome **At the end of the course, student should be able to . . .**	Teach. Hours	Instr Method	Assessment Method	Blooms' Level
1	CO1	Analyze the concepts of MOS transistor theory to understand the characteristics of MOSFETs.	10	Lecture	CIA / Assignment	L2 Understand
2	CO2	Apply the concepts of MOSFETs to construct logic gates and develop stick diagrams, layout.	10	Lecture / Video	CIA / Assignment	L3 Apply
3	CO3	Analyze the delay characteristics of CMOS circuits using basic circuit concepts	10	Lecture	CIA / Assignment	L3 Apply L4 Analyze
4	CO4	Design a sub-system and analyze its architecture issues and understand the FPGA Architecture.	10	Lecture	CIA / Assignment	L3 Apply L4 Analyze
5	CO5	Understand the memory and testablility issues	10	Lecture	CIA / Assignment	L3 Apply
-	-	**Total**	**50**	-	-	**L2-L3**

2. Course Applications

Write 1 or 2 applications per CO.
Students should be able to employ / apply the course learnings to . . .

Modules	Application Area Compiled from Module Applications.	CO	Level
1	Fabrication process is used for manufacture of all IC's	CO1	L2

2	Back-end VLSI design for preparing the mask	CO2	L3
3	Delay estimation in the IC design.	CO3	L3
4	Designing processors	CO4	L4
5	Testing of IC's	CO5	L2

3. Articulation Matrix

CO – PO Mapping with mapping level for each CO-PO pair, with course average attainment.

-	-	Course Outcomes	Program Outcomes														-
Modules	CO.#	**At the end of the course student should be able to . . .**	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3	Level
1	Analyze the characteristic of the MOSFET	2	2	2														
2	Construct and develop the logic gates and its layout and the stick diagrams.	3	2	2	2								2					
3	Estimate the delay for the given physical structure.	3	2	2	2								2					
4	Design a sub-system and analyze its architecture issues.	3	3	2	2								2					
5	Understand the FPGA architecture and testablility issues	3	2	2									2					
-	**17EC63.**	2.8	**2.2**	**2**	**2**								**2**					**-**
-	*PO, PSO*	*1.Engineering Knowledge; 2.Problem Analysis; 3.Design / Development of Solutions; 4.Conduct Investigations of Complex Problems; 5.Modern Tool Usage; 6.The Engineer and Society; 7.Environment and Sustainability; 8.Ethics; 9.Individual and Teamwork; 10.Communication; 11.Project Management and Finance; 12.Life-long Learning; S1.Software Engineering; S2.Data Base Management; S3.Web Design*																

4. Curricular Gap and Content

Topics & contents not covered (from A.4), but essential for the course to address POs and PSOs.

Modules	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1	Simulation of MOS Circuits	Seminar		Subject handing faculty	PO5

C. COURSE ASSESSMENT

1. Course Coverage

Assessment of learning outcomes for Internal and end semester evaluation.

Modules	Title	Teach. Hours	No. of question in Exam						CO	Levels
			CIA-1	CIA-2	CIA-3	Asg	Extra Asg	SEE		
1.	Introduction, Fabrication	10	2	-	-	1	1	2	CO1	L2
2.	MOS and BiCMOS Circuit Design	10	2	-	-	1	1	2	CO2	L3

	Processes, Basic circuit concepts									
3.	Scaling of MOS Circuits, Subsystem Design Processes	10	-	2	-	1	1	2	CO3	L3
4.	Subsystem Design, FPGA Based Systems	10	-	2	-	1	1	2	CO4	L3
5.	Memory, Registers and Aspects of system Timing, Testing and Verification	10	-	-	4	1	1	2	CO5	L2
-	**Total**	**50**	**4**	**4**	**4**	**5**	**5**	**10**	**-**	**-**

2. Continuous Internal Assessment (CIA)

Assessment of learning outcomes for Internal exams. Blooms Level in last column shall match with A.2.

Modules	Evaluation	Weightage in Marks	CO	Levels
1, 2	CIA Exam – 1	30	CO1, CO2	L2-L3
3, 4	CIA Exam – 2	30	CO3, CO4	L2-L3
5	CIA Exam – 3	30	CO5	L2-L3
1, 2	Assignment - 1	10	CO1, CO2	L2-L3
3, 4	Assignment - 2	10	CO3, CO4	L2-L3
5	Assignment - 3	10	CO5	L2-L3
1, 2	Seminar - 1		-	-
3, 4	Seminar - 2		-	-
5	Seminar - 3		-	-
1, 2	Quiz - 1		-	-
3, 4	Quiz - 2		-	-
5	Quiz - 3		-	-
1 - 5	Other Activities – Mini Project	-		
	Final CIA Marks	**40**	**-**	**-**

D1. TEACHING PLAN - 1

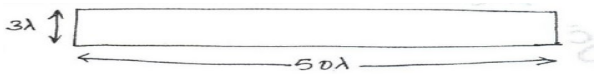
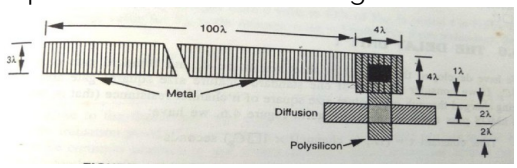
Module - 1

Title:	Introduction	Appr Time:	10 Hrs
a	***Course Outcomes***	**CO**	**Blooms**
	Analyze the characteristic of the MOSFET	CO1	**L2**
b	***Course Schedule***	-	-
Class No	**Portion covered per hour**	**-**	**-**
1.	A Brief History.	CO1	L2
2.	MOS Transistors.	CO1	L2
3.	MOS Transistor Theory.	CO1	L2
4.	Ideal I-V Characteristics.	CO1	L2
5.	Non-ideal I-V Effects.	CO1	L2
6.	DC Transfer Characteristics.	CO1	L2
7.	**Fabrication:** nMOS Fabrication.	CO1	L2
8.	CMOS Fabrication [P-well process, N-well process, Twin tub process].	CO1	L2

9.	CMOS Fabrication continued..	CO1	L2
10.	BiCMOS Technology	CO1	L2
d	**Review Questions**		
-			
1.	What do you mean by static load inverters? Derive the output voltage for pseudo Inverter by discussing its dc characteristics.		
2.	Derive the CMOS inverter DC characteristics graphically from p device and n device characteristics and show all operating regions.	CO1	L2
3.	Explain the nMOS enhancement mode transistor operation for different values of Vgs and Vds .	CO1	L2
4.	Explain the fabrication steps of CMOS p-well process with neat diagram and write the mask sequence.	CO1	L2
5.	What are the advantages of BiCMOS process over CMOS technology.	CO1	L2
6.	With Suitable diagrams explain the three regions of operation of Enhancement mode NMOS transistor.	CO1	L2
7.	With Suitable diagrams explain the three regions of operation of depletion mode NMOS transistor.	CO1	L2
8.	With Suitable diagrams explain the three regions of operation of Enhancement mode PMOS transistor.	CO1	L2
9.	With Suitable diagrams explain the three regions of operation of depletion mode PMOS transistor.	CO1	L2
10.	Using graphical approach explain the DC characteristics of a CMOS inverter.	CO1	L2
11.	Differentiate between CMOS and Bipolar technologies.	CO1	L2
12.	With neat sketches explain the CMOS P-well process steps to fabricate a CMOS inverter.	CO1	L2
13.	With neat sketches explain the CMOS N-well process steps to fabricate a CMOS inverter.	CO1	L2
14.	With neat sketches explain the CMOS Twin tub process steps to fabricate a CMOS inverter.	CO1	L2
15.	Derive a first order expression relating the current and voltage (I-V) for an NMOS transistor in Linear region.	CO1	L2
16.	Explain any two non ideal I-V effects in a MOS device.	CO1	L2
e	**Experiences**	-	-
1		CO1	L2
2			

Module – 2

Title:	MOS and BiCMOS Circuit Design Process	Appr Time:	10 Hrs
a	***Course Outcomes***	**CO**	**Blooms**
-	Construct and develop the logic gates and its layout and the stick diagrams.	CO2	**L2-L3**
b	***Course Schedule***	-	-
Class No	**Portion covered per hour**	**-**	**-**
11.	MOS Layers	CO2	L2-L3
12.	Stick Diagrams,	CO2	L2-L3
13.	Design Rules and Layout.	CO2	L2-L3
14.	Layout continued.	CO2	L2-L3
15.	Layout continued.	CO2	L2-L3
16.	**Basic Circuit Concepts:** Sheet Resistance, Area Capacitances of	CO2	L2-L3

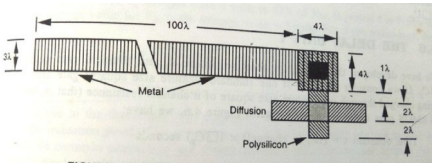
	Layers.		
17.	Standard Unit of Capacitance.	CO2	L2-L3
18.	Some Area Capacitance Calculations.	CO2	L2-L3
19.	Delay Unit, Inverter Delays.	CO2	L2-L3
20.	Driving Large Capacitive Loads.	CO2	L2-L3
c	**Application Areas**	**-**	**-**
-	Students should be able employ / apply the Module learnings to . . .	-	-
1	Draw mask for various digital circuits for IC designing.	CO2	
d	**Review Questions**	-	-
-			
1.	Explain lambda based design rules with neat diagram.	CO2	L2
2.	Draw the circuit and stick diagram for nMOS and CMOS implementation of Boolean expression y= a+b	CO2	L3
3.	What do you mean by lambda based design rules? List the lambda based design rules for CMOS Technology.	CO2	L2
4.	Explain lambda based design rules for wires, transistors and contact cuts.	CO2	L2
5.	Draw the schematic, stick diagram and layout for a CMOS NAND gate.	CO2	L3
6.	Draw the schematic, stick diagram and layout for a CMOS NOR gate.	CO2	L3
7.	Draw the schematic, stick diagram and layout for a CMOS OR gate.	CO2	L3
8.	Draw the schematic, stick diagram and layout for a CMOS AND gate.	CO2	L3
9.	Draw the schematic, stick diagram and layout for a CMOS XOR gate.	CO2	L3
10.	Draw the schematic, stick diagram and layout for a CMOS XNOR gate.	CO2	L3
11.	Calculate the capacitance in Cg for the given metal layer shown in the Fig Q4(a), if feature size=5μm and relative value of metal to substrate =0.075.  Fig Q4(a)	CO2	L3
12.	Define sheet resistance Rs and standard unit of capacitance (□Cg). Calculate the on resistance of 4:1 nMOS inverter with Rs=10k/□, Zpu=8λ/2λ, Zpd=2λ/2λ. Also estimate the total power dissipated if VDD=5V.	CO2	L2
13.	Derive the expression for sheet resistance Rs.	CO2	L2
14.	Calculate the capacitance of the structure given below in Figure 4(b)  **Figure 4(b)**	CO2	L3
15.	Derive an expression for the estimation of CMOS inverter Delay.	CO2	L3
e	**Experiences**	-	-
1			
2			

E1. CIA EXAM – 1

a. Model Question Paper - 1

Crs Code:	17EC63	Sem:	VI	Marks:	30	Time:	75 minutes

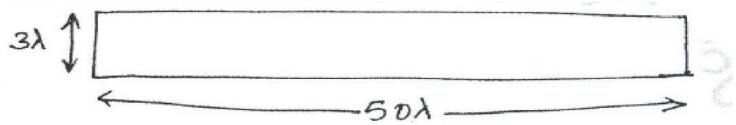
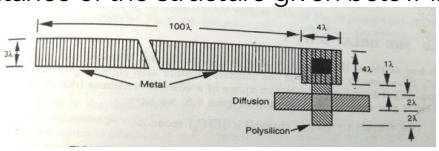
Course:		VLSI Design			
-	**-**	**Note: Answer any 1 question from each Module.**	**Marks**	**CO**	**Level**
		MODULE 1			
1	a	Derive the CMOS inverter DC characteristics graphically from p device	8	CO1	L2

		and n device characteristics and show all operating regions.			
	b	Explain the nMOS enhancement mode transistor operation for different values of Vgs and Vds .	7	CO1	L2
		OR			
2	a	Differentiate between CMOS and Bipolar technologies.	8	CO2	L2
	b	With neat sketches explain the CMOS P-well process steps to fabricate a CMOS inverter.	7	CO2	L2
		MODULE 2			
3	a	Explain lambda based design rules for wires, transistors and contact cuts.	8	C03	L2
	b	Draw the schematic, stick diagram and layout for a CMOS NAND gate.	7	C03	L3
		OR			
4	a	Calculate the capacitance of the structure given below in Figure 4(a)  **Figure 4(a)**	8	C04	L3
	b	Define sheet resistance Rs and standard unit of capacitance (ɒCg). Calculate the on resistance of 4:1 nMOS inverter with Rs=10k/ɒ, Zpu=8λ/2λ, Zpd=2λ/2λ. Also estimate the total power dissipated if VDD=5V.	7	C04	L3

b. Assignment -1

Model Assignment Questions							
Crs Code:	17EC63	Sem:	VI	Marks:	30	Time:	90-120 minutes
Course:	VLSI Design						

SNo	Assignment Description	Marks	CO	Level
1.	What do you mean by static load inverters? Derive the output voltage for pseudo Inverter by discussing its dc characteristics.	8	CO1	L2
2.	Derive the CMOS inverter DC characteristics graphically from p device and n device characteristics and show all operating regions.	8	CO1	L2
3.	Explain the nMOS enhancement mode transistor operation for different values of Vgs and Vds .	6	CO1	L2
4.	Explain the fabrication steps of CMOS p-well process with neat diagram and write the mask sequence.	6	CO1	L2
5.	What are the advantages of BiCMOS process over CMOS technology.	4	CO1	L2
6.	With Suitable diagrams explain the three regions of operation of Enhancement mode NMOS transistor.	7	CO1	L2
7.	With Suitable diagrams explain the three regions of operation of depletion mode NMOS transistor.	7	CO1	L2
8.	With Suitable diagrams explain the three regions of operation of Enhancement mode PMOS transistor.	7	CO1	L2
9.	With Suitable diagrams explain the three regions of operation of depletion mode PMOS transistor.	7	CO1	L2
10.	Using graphical approach explain the DC characteristics of a CMOS inverter.	5	CO1	L2
11.	Differentiate between CMOS and Bipolar technologies.	4	CO1	L2
12.	With neat sketches explain the CMOS P-well process steps to fabricate a CMOS inverter.	6	CO1	L2
13.	With neat sketches explain the CMOS N-well process steps to fabricate a CMOS inverter.	6	CO1	L2
14.	With neat sketches explain the CMOS Twin tub process steps to fabricate a CMOS inverter.	6	CO1	L2
15.	Derive a first order expression relating the current and voltage (I-V) for an NMOS transistor in Linear region.	6	CO1	L2

16.	Explain only two non ideal I-V effects in a MOS device.	4	CO1	L2
17.	Explain lambda based design rules with neat diagram.	6	CO2	L2
18.	Draw the circuit and stick diagram for nMOS and CMOS implementation of Boolean expression y= a+b	10	CO2	L3
19.	What do you mean by lambda based design rules? List the lambda based design rules for CMOS Technology.	7	CO2	L2
20.	Explain lambda based design rules for wires, transistors and contact cuts.	8	CO2	L2
21.	Draw the schematic, stick diagram and layout for a CMOS NAND gate.	9	CO2	L3
22.	Draw the schematic, stick diagram and layout for a CMOS NOR gate.	9	CO2	L3
23.	Draw the schematic, stick diagram and layout for a CMOS OR gate.	9	CO2	L3
24.	Draw the schematic, stick diagram and layout for a CMOS AND gate.	9	CO2	L3
25.	Draw the schematic, stick diagram and layout for a CMOS XOR gate.	9	CO2	L3
26.	Draw the schematic, stick diagram and layout for a CMOS XNOR gate.	9	CO2	L3
27.	Calculate the capacitance in Cg for the given metal layer shown in the Fig Q4(a), if feature size=5µm and relative value of metal to substrate =0.075.  Fig Q4(a)	8	CO2	L3
28.	Define sheet resistance Rs and standard unit of capacitance (□Cg). Calculate the on resistance of 4:1 nMOS inverter with Rs=10k/□, Zpu=8λ/2λ, Zpd=2λ/2λ. Also estimate the total power dissipated if VDD=5V.	8	CO2	L3
29.	Derive the expression for sheet resistance Rs.	4	CO2	L2
30.	Calculate the capacitance of the structure given below in Figure 4(b)  **Figure 4(b)**	6	CO2	L3
31.	Derive an expression for the estimation of CMOS inverter Delay.	6	CO2	L2

D2. TEACHING PLAN - 2

Module – 3

Title:	**Scaling of MOS Circuits**	Appr Time:	10 Hrs
a	***Course Outcomes***	**CO**	**Blooms**
-	Estimate the delay for the given physical structure.	CO3	**L3**
b	***Course Schedule***		
Class No	**Portion covered per hour**	**-**	
21.	Scaling Models	CO3	L2
22.	Scaling Factors for Device Parameters.	CO3	L2
23.	**Subsystem Design Processes:** Some General considerations.	CO3	L2
24.	An illustration of Design Processes.	CO3	L2
25.	**Illustration of the Design Processes**- Regularity.	CO3	L2
26.	Design of an ALU Subsystem.	CO3	L3
27.	Design of an ALU Subsystem continued.	CO3	L3
28.	The Manchester Carry-chain.	CO3	L3
29.	Adder Enhancement Techniques.	CO3	L3
30.	Adder Enhancement	CO3	L3

	Techniques.		
c	**Application Areas**	**-**	**-**
-	Students should be able employ / apply the Module learnings to . . .	-	-
	Design of Microprocessors and controllers	CO3	L3
d	**Review Questions**	-	-
-	The attainment of the module learning assessed through following questions	-	-
1.	Obtain the scaling factor for the following device parameters: (I) Gate Capacitance (II) Gate Area (III) Saturation Current (Idss) (IV) Channel Resistance (Ron) (V) Max Operating Frequency (fo) (VI) Power Dissipation per gate (Pg) (VII) Current density (J) (VIII) Gate delay (Td).	CO3	L3
2.	With a neat diagram explain 4x4 Barrel shifter.	CO3	L2
3.	Explain the general arrangement of a 4 bit ALU.	CO3	L2
4.	Explain in detail any One Adder Enhancement technique.	CO3	L2
5.	Find the scaling factors for: i) Saturation current ii) Current density iii) Power dissipation/unit area iv) Maximum operating frequency	CO3	L3
6.	Design a 4 bit ALU to implement addition, subtraction, EX-OR, EX-NOR, OR and AND operations.	CO3	L3
7.	With a neat diagram, explain 4x4 barrel shifter.	CO3	L2
8.	Describe Manchester Carry-chain.	CO3	L2
e	**Experiences**	-	-
1			
2			

Module – 4

Title:	CMOS Subsystem Design	Appr Time:	10 Hrs
a	***Course Outcomes***	**CO**	**Blooms**
-	At the end of the topic the student should be able to . . .	-	**Level**
	Design a sub-system and analyze its architecture issues and understand the FPGA Architecture.	CO4	L3
b	***Course Schedule***		
Class No	**Portion covered per hour**	**-**	**-**
31.	Some Architectural Issues.	CO4	L2
32.	Switch Logic.	CO4	L3
33.	Gate(restoring) Logic.	CO4	L3
34.	Parity Generators.	CO4	L3
35.	Multiplexers.	CO4	L3
36.	The Programmable Logic Array (PLA).	CO4	L3
37.	(**FPGA Based Systems:** Introduction, Basic concepts.	CO4	L2
38.	Digital design and FPGA‘s.	CO4	L2
39.	FPGA based System design.	CO4	L2
40.	FPGA architecture, Physical design for FPGA‘s.	CO4	L2
c	**Application Areas**	**-**	**-**
-	Students should be able employ / apply the Module learnings to . . .	-	-

	Microprcossor Design	CO4	L3
d	**Review Questions**	-	-
-	The attainment of the module learning assessed through following questions	-	-
1.	Discuss the architectural issues related to VLSI subsystem design.	CO4	L2
2.	Explain Pseudo nMOS logic for NAND gate and Inverter.	CO4	L2
3.	Discuss the architectural issues to be followed in the design of a VLSI subsystem.	CO4	L2
4.	Explain in detail the Generic Structure of an FPGA fabric.	CO4	L2
5.	Explain switch logic implementation of a 4x4 four way multiplexer.	CO4	L2
6.	Explain Parity generator with basic block diagram and stick diagram.	CO4	L2
7.	Explain Field Programmable Gate Array architectures.	CO4	L2
8.	Explain the Structured Design approach for the implementation of a Parity Generator with relevant stick diagram.	CO4	L2
9.	Explain Dynamic CMOS logic with an example.	CO4	L2
10.	Discuss the programmable logic array with its structure and floor plan	CO4	L2
11.	Discuss the design of data selectors	CO4	L2
12.	Discuss the FPGA abstractions with a diagram.	CO4	L2
e	**Experiences**	-	-
1		CO7	L2
2			

E2. CIA EXAM – 2

a. Model Question Paper - 2

Crs Code:	17EC63	Sem:	6	Marks:	20	Time:	75 minutes
Course:	VLSI Design						

-	-	**Note: Answer any 1 question from each Module.**	**Marks**	**CO**	**Level**
		Module 1			
1	a	Find the scaling factors for: i) Saturation current ii) Current density iii) Power dissipation/unit area iv) Maximum operating frequency	8	CO5	L3
	b	Explain the general arrangement of a 4 bit ALU.	7	CO6	L2
		OR			
2	a	With a neat diagram, explain 4x4 barrel shifter.	8	CO6	L2
	b	Discribe Manchester Carry-chain.	7	CO6	L2
		Module 2			
3	a	Explain switch logic implementation of a 4x4 four way multiplexer.	8	CO7	L2
	b	Explain Parity generator with basic block diagram and stick diagram.	7	CO7	L2
		OR			
4	a	Discuss the design of data selectors	8	CO8	L2
	b	Discuss the FPGA abstractions with a diagram.	7	CO8	L2

b. Assignment – 2

Model Assignment Questions							
Crs Code:	17EC63	Sem:	6	Marks:		Time:	
Course:	VLSI Design						

SNo	Assignment Description	Marks	CO	Level
1.	Obtain the scaling factor for the following device parameters: (I) Gate Capacitance (II) Gate Area (III) Saturation Current (Idss) (IV) Channel Resistance (Ron) (V) Max Operating Frequency (fo) (VI) Power Dissipation per gate (Pg) (VII) Current density (J) (VIII) Gate delay (Td).	8	CO3	L3
2.	With a neat diagram explain 4x4 Barrel shifter.	8	CO3	L2
3.	Explain the general arrangement of a 4 bit ALU.	8	CO3	L2
4.	Explain in detail any One Adder Enhancement technique.	8	CO3	L2
5.	Find the scaling factors for: i) Saturation current ii) Current density iii) Power dissipation/unit area iv) Maximum operating frequency	8	CO3	L3
6.	Design a 4 bit ALU to implement addition, subtraction, EX-OR, EX-NOR, OR and AND operations.	8	CO3	L3
7.	With a neat diagram, explain 4x4 barrel shifter.	8	CO3	L2
8.	Describe Manchester Carry-chain.	8	CO3	L2
9.	Discuss the architectural issues related to VLSI subsystem design.	8	CO4	L2
10.	Explain Pseudo nMOS logic for NAND gate and Inverter.	8	CO4	L2
11.	Discuss the architectural issues to be followed in the design of a VLSI subsystem.	5	CO4	L2
12.	Explain in detail the Generic Structure of an FPGA fabric.	7	CO4	L2
13.	Explain switch logic implementation of a 4x4 four way multiplexer.	4	CO4	L2
14.	Explain Parity generator with basic block diagram and stick diagram.	8	CO4	L2
15.	Explain Field Programmable Gate Array architectures.	8	CO4	L2
16.	Explain the Structured Design approach for the implementation of a Parity Generator with relevant stick diagram.	8	CO4	L2
17.	Explain Dynamic CMOS logic with an example.	8	CO4	L2
18.	Discuss the programmable logic array with its structure and floor plan	5	CO4	L2
19.	Discuss the design of data selectors	5	CO4	L2
20.	Discuss the FPGA abstractions with a diagram.	6	CO4	L2

D3. TEACHING PLAN - 3

Module – 5

Title:	**Memory, Registers and Aspects of system Timing**	Appr Time:	10 Hrs
a	***Course Outcomes***	**CO**	**Blooms**
-	At the end of the topic the student should be able to . . .	-	**Level**
	Understand the memory and testablility issues	CO5	L2

b	***Course Schedule***	-	-
Class No	**Portion covered per hour**	**-**	**-**
41.	System Timing Considerations.	CO5	L2
42.	Some commonly used Storage/Memory elements.	CO5	L2
43.	Some commonly used Storage/Memory elements continued.	CO5	L2
44.	Some commonly used Storage/Memory elements continued.	CO5	L2
45.	**Testing and Verification:** Introduction.	CO5	L2
46.	Logic Verification.	CO5	L2
47.	Logic Verification Principles.	CO5	L2
48.	Manufacturing Test Principles.	CO5	L2
49.	Design for testability.	CO5	L2
50.	Design for testability continued.	CO5	L2
c	**Application Areas**	**-**	**-**
-	Students should be able employ / apply the Module learnings to . . .	-	-
	Test the IC	CO5	L3
d	**Review Questions**	-	-
-	The attainment of the module learning assessed through following questions	-	-
1.	Explain 3 transistor dynamic RAM cell.	CO5	L2
2.	Write a note on testability and testing.	CO5	L2
3.	Explain the scan design techniques.	CO5	L2
4.	Demonstrate write operation & read operation for four transistor dynamic and six transistor static CMOS memory cell.	CO5	L3
5.	Explain 3-Transistor Dynamic RAM cell with Schematic and stick diagram.	CO5	L2
6.	List the System timing Considerations.	CO5	L1
7.	Explain any two fault models in combinational circuits.	CO5	L2
8.	Explain Pseudo-Static RAM cell (CMOS) with schematic and stick diagram.	CO5	L2
9.	Write short notes on I) Observability and Controllability II) Built in Self Test (BIST)	CO5	L2
10.	Explain three transistor DRAM with its diagram and stick diagram.	CO5	L2
11.	Discuss the ASM chart for JK flip flop with its NAND and logic arrangement.	CO5	L2
12.	Explain logic verification process with its functional equivalence diagram.	CO5	L2
13.	Discuss the design for manufacturability.	CO5	L2
14.	Discuss the Ad-hoc testing.	CO5	L2
e	**Experiences**	-	-
1			
2			

E3. CIA EXAM – 3

a. Model Question Paper - 3

Crs Code:	17EC63	Sem:	6	Marks:	30	Time:	75 minutes
Course:	VLSI Design						

-	-	**Note: Answer any 2 questions, each carry equal marks.**	**Marks**	**CO**	**Level**
1	a	Explain 3-Transistor Dynamic RAM cell with Schematic and stick diagram.	8	CO5	L2
	b	Explain Pseudo-Static RAM cell (CMOS) with schematic and stick diagram.	7	CO5	L2
		or			

2	a	Explain the scan design techniques.	8	CO5	L2
	b	Discuss the ASM chart for JK flip flop with its NAND and logic arrangement.	7	CO5	L2
3	a	Explain logic verification process with its functional equivalence diagram.	8	CO5	L2
	b	Discuss the design for manufacturability.	7	CO5	L2
		or			
4	a	Write a note on testability and testing.	8	CO5	L2
	b	Discuss the Ad-hoc testing.	7	CO5	L2

b. Assignment – 3

Model Assignment Questions							
Crs Code:	17EC63	Sem:	6	Marks:	5 / 10	Time:	90 – 120 minutes
Course:	VLSI Design						

SNo	Assignment Description	Marks	CO	Level
1.	Explain 3 transistor dynamic RAM cell.	8	CO5	L2
2.	Write a note on testability and testing.	8	CO5	L2
3.	Explain the scan design techniques.	8	CO5	L2
4.	Demonstrate write operation & read operation for four transistor dynamic and six transistor static CMOS memory cell.	8	CO5	L3
5.	Explain 3-Transistor Dynamic RAM cell with Schematic and stick diagram.	6	CO5	L2
6.	List the System timing Considerations.	4	CO5	L1
7.	Explain any two fault models in combinational circuits.	6	CO5	L2
8.	Explain Pseudo-Static RAM cell (CMOS) with schematic and stick diagram.	8	CO5	L2
9.	Write short notes on I) Observability and Controllability II) Built in Self Test (BIST)	8	CO5	L2
10.	Explain three transistor DRAM with its diagram and stick diagram.	7	CO5	L2
11.	Discuss the ASM chart for JK flip flop with its NAND and logic arrangement.	9	CO5	L2
12.	Explain logic verification process with its functional equivalence diagram.	6	CO5	L2
13.	Discuss the design for manufacturability.	6	CO5	L2
14.	Discuss the Ad-hoc testing.	4	CO5	L2

F. EXAM PREPARATION

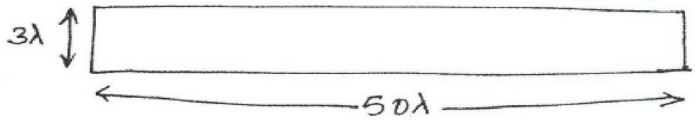
1. University Model Question Paper

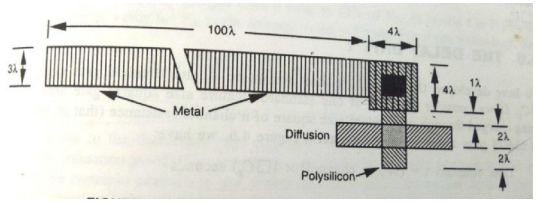
Course:	VLSI Design					Month / Year	JULY /2020	
Crs Code:	17ec63	Sem:	6	Marks:	100	Time:	180 minutes	
-	**Note**	Answer any FIVE full questions, choosing ONE full question from each module				**Marks**	**CO**	**Level**
1	a	Derive the CMOS inverter DC characteristics graphically from p device and n device characteristics and show all operating regions.				8	CO1	L2
	b	With Suitable diagrams explain the three regions of operation of depletion mode NMOS transistor.				8	CO1	L2
		or						
2	a	With neat sketches explain the CMOS Twin tub process steps to fabricate				9	CO2	L2

		a CMOS inverter.			
	b	With neat diagram discuss the nMOS fabrication process steps.	7	CO2	L2
3	a	Discuss the CMOS design style with a diagram.	5	CO3	L2
	b	Draw the stick diagram for the following using CMOS logic (i) Y=A+B+C (ii) 2 i/p NAND gate.	5	CO3	L3
	c	Discuss the different contact cuts with an example to each	6	CO3	L2
		or			
4	a	With a diagram derive an expression for sheet resistance and mention the Rs values of metal, p and n transistor channels for 5 um technology.	5	CO4	L2
	b	Derive an equation for rise time and fall time with respect to CMOS inverter.	8	CO4	L2
	c	Draw the circuit and stick diagram for 2 i/p NOR gate using CMOS logic.	3	CO3	L3
5	a	Explain the constant field, constant voltage scaling models with a diagram and scaling effect table.	6	CO5	L2
	b	Discuss the problems associated in VLSI design. How do you reduce them?	5	CO5	L2
	c	Discuss the different bus architectures.	5	CO5	L2
		or			
6	a	Discuss the design of 4-bit adder.	7	CO6	L2
	b	With relevant diagram discuss Manchester carry chain operation.	5	CO6	L2
	c	Explain the carry select adder with a diagram.	4	CO6	L2
7	a	Discuss the programmable logic array with its structure and floor plan	5	CO7	L2
	b	Discuss the architectural issues related to VLSI subsystem design.	6	CO7	L2
	c	Discuss the design of data selectors.	5	CO7	L2
		or			
8	a	Explain the architecture of field programmable gate array	10	CO8	L2
	b	Discuss the FPGA abstractions with a diagram.	6	CO8	L2

2. SEE Important Questions

Course:	VLSI Design					Month / Year	June /2020
Crs Code:	17EC63	Sem:	6	Marks:	100	Time:	180 minutes

	Note	Answer all FIVE full questions. All questions carry equal marks.	-	-	
Module	Qno.	Important Question	Marks	CO	Year
1	1	Derive the CMOS inverter DC characteristics graphically from p device and n device characteristics and show all operating regions.	8	CO1	L2
	2	Explain the nMOS enhancement mode transistor operation for different values of Vgs and Vds .	6	CO1	L2
	3	Explain the fabrication steps of CMOS p-well process with neat diagram and write the mask sequence.	6	CO2	L2
	4	What are the advantages of BiCMOS process over CMOS technology.	4	CO2	L2
	5	With Suitable diagrams explain the three regions of operation of Enhancement mode NMOS transistor.	7	CO1	L2
2	1	Draw the schematic, stick diagram and layout for a CMOS XNOR gate.	9	CO3	L3
	2	Calculate the capacitance in Cg for the given metal layer shown in the Fig Q4(a), if feature size=5μm and relative value of metal to substrate =0.075.  Fig Q4(a)	8	CO4	L3
	3	Define sheet resistance Rs and standard unit of capacitance (◻Cg). Calculate the on resistance of 4:1 nMOS inverter with Rs=10k/◻, Zpu=8λ/	8	CO4	L3

		2ƛ, Zpd=2ƛ/2ƛ. Also estimate the total power dissipated if VDD=5V.			
	4	Derive the expression for sheet resistance Rs.	4	CO4	L2
	5	Calculate the capacitance of the structure given below in Figure 4(b)  **Figure 4(b)**	6	CO4	L3
3	1	Explain in detail any One Adder Enhancement technique.	8	CO6	L2
	2	Find the scaling factors for: i) Saturation current ii) Current density iii) Power dissipation/unit area iv) Maximum operating frequency	8	CO5	L3
	3	Design a 4 bit ALU to implement addition, subtraction, EX-OR, EX-NOR, OR and AND operations.	8	CO6	L3
	4	With a neat diagram, explain 4x4 barrel shifter.	8	CO6	L2
	5	Describe Manchester Carry-chain.	8	CO6	L2
4	1	Explain the Structured Design approach for the implementation of a Parity Generator with relevant stick diagram.	8	CO7	L2
	2	Explain Dynamic CMOS logic with an example.	8	CO7	L2
	3	Discuss the programmable logic array with its structure and floor plan	5	CO8	L2
	4	Discuss the design of data selectors	5	CO8	L2
	5	Discuss the FPGA abstractions with a diagram.	6	CO8	L2
5	1	Explain 3 transistor dynamic RAM cell.	8	CO9	L2
	2	Write a note on testability and testing.	8	CO10	L2
	3	Explain the scan design techniques.	8	CO10	L2
	4	Demonstrate write operation & read operation for four transistor dynamic and six transistor static CMOS memory cell.	8	CO9	L3
	5	Explain 3-Transistor Dynamic RAM cell with Schematic and stick diagram.	6	CO9	L2

Course Outcome Computation

Academic Year:

Odd / Even semester

INTERNAL TEST	**T1**						**T2**						**T3**			
Course Outcome																
QUESTION NO	**Q1**	**LV**	**Q2**	**LV**	**Q3**	**LV**	**Q1**	**LV**	**Q2**	**LV**	**Q3**	**LV**	**Q1**	**LV**	**Q2**	**LV**
MAX MARKS																
USN-1																
USN-2																
USN-3																
USN-4																
USN-5																
USN-6																
Average CO Attainment																

LV Threshold : 3:>60%, 2:>=50% and <=60%, 1: <=49%
CO1 Computation :(2+2+2+3)/4 = 10/4=2.5

PO Computation

Program Outcome	PO1	PO3	PO3	PO1	PO12	PO12	PO6	PO1
Weight of CO - PO	3	1	3	2	2	3	3	1
Course Outcome	CO1	CO2	CO3	CO4	CO5	CO6	CO7	CO8

Test/Quiz/ Lab	T1						T2						T3			
QUESTION NO	Q1	LV	Q2	LV	Q3	LV	Q1	LV	Q2	LV	Q3	LV	Q1	LV	Q2	LV
MAX MARKS	10	-	10	-	10	-	10	-	10	-	10	-	10	-	10	-
USN-1																
USN-2																
USN-3																

USN-4 USN-5 USN-6
Average CO Attainment