Ref No:

Sri Krishna Institute of Technology,
Bangalore

COURSE PLAN

Academic Year 2019-2020

Program:	B.E
Semester :	VI
Course Code:	17EC62
Course Title:	ARM Microcontroller & Embedded System
Credit / L-T-P:	4/4-0-0
Total Contact Hours:	50
Course Plan Author:	M.Nagaraja

Academic Evaluation and Monitoring Cell

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A. COURSE INFORMATION

1. Course Overview

Degree:	B.E	Program:	UG
Semester:	VI	Academic Year:	2019-20
Course Title:	ARM Microcontroller & Embedded System	Course Code:	17EC62
Credit / L-T-P:	4/4-0-0	SEE Duration:	180 minutes
Total Contact Hours:	50	SEE Marks:	60
CIA Marks:	30	Assignment	10
Course Plan Author:	M.Nagaraja	Sign ..	
Checked By:		Sign ..	
CO Targets	CIA Target :20	SEE Target:	65

Note: Define CIA and SEE % targets based on previous performance.

2. Course Content

Content / Syllabus of the course as prescribed by University or designed by institute.

Module	Content	Teaching Hours	Blooms Learning Levels
1	**ARM-32 bit Microcontroller:** Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, Debugging support, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence.	10	L2,L3
2	**ARM Cortex M3 Instruction Sets and Programming:** Assembly basics, Instruction list and description, Useful instructions, Memory mapping, Bit-band operations and CMSIS, Assembly and C language Programming	10	L2,L3
3	**Embedded System Components:** Embedded Vs General computing system, Classification of Embedded systems, Major applications and purpose of ES. Core of an Embedded System including all types of processor/controller, Memory, Sensors, Actuators, LED, 7 segment LED display, Optocoupler, Relay, Piezo buzzer, Push button switch, Communication Interface (onboard and external types), Embedded firmware, Other system components.	10	L2,L3,L4
4	**Embedded System Design Concepts:** Characteristics and Quality Attributes of Embedded Systems, Operational and non-operational quality attributes, Embedded 86 Systems-Application and Domain specific, Hardware Software Co-Design and Program Modelling (excluding UML), Embedded firmware design and development (excluding C language).	10	L2,L3,L4
5	**RTOS and IDE for Embedded System Design:** Operating System basics, Types of operating systems, Task, process and threads (Only POSIX Threads with an example program), Thread preemption, Preemptive Task scheduling techniques, Task Communication, Task synchronization issues – Racing and Deadlock, Concept of Binary and counting semaphores (Mutex example without any program), How to choose an RTOS, Integration and testing of Embedded hardware and firmware, Embedded system Development Environment – Block diagram (excluding Keil), Disassembler/decompiler,	10	L2,L3,L4

	simulator, emulator and debugging techniques		
-	**Total**		

3. Course Material

Books & other material as recommended by university (A, B) and additional resources used by course teacher (C).
1. Understanding: Concept simulation / video ; one per concept ; to understand the concepts ; 15 – 30 minutes
2. Design: Simulation and design tools used – software tools used ; Free / open source
3. Research: Recent developments on the concepts – publications in journals; conferences etc.

Modules	Details	Chapters in book	Availability
A	**Text books (Title, Authors, Edition, Publisher, Year.)**	**-**	**-**
	Joseph Yiu, "The Definitive Guide to the ARM Cortex-M3", 2nd Edition, Newnes, (Elsevier), 2010.	In Lib	
	Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education Private Limited, 2nd Edition.	In Lib	
B	**Reference books (Title, Authors, Edition, Publisher, Year.)**	**-**	**-**
C	**Concept Videos or Simulation for Understanding**	**-**	**-**
1	https://www.youtube.com/watch?v=-o0ybJmyT2U https://www.youtube.com/watch?v=x0gH5JGNIKg	Available	
2	https://www.youtube.com/watch?v=15z_vn4H41U&list=PL77-op_SRaiF2xlczKtEWqkB-5iuNBN5-	Available	
3	https://www.youtube.com/watch?v=bsNvMc6JD10	Available	
4	https://www.youtube.com/watch?v=8grRV-iBYts	Available	
5	https://www.youtube.com/watch?v=3V9eqvkMzHA	Available	
D	**Software Tools for Design**	**-**	**-**
	KEIL		
E	**Recent Developments for Research**	**-**	**-**
F	**Others (Web, Video, Simulation, Notes etc.)**	**-**	**-**
1			

4. Course Prerequisites

Refer to GL01. If prerequisites are not taught earlier, GAP in curriculum needs to be addressed. Include in Remarks and implement in B.5.
Students must have learnt the following Courses / Topics with described Content . . .

Modules	Course Code	Course Name	Topic / Description	Sem	Remarks	Blooms Level
1	15EC563	8051 Microcontroller	Architecture, instruction set, programming	5		L3
1	15EC42	Microprocessors	Architecture, instruction set, programming	4		L3
3	15EC553	Operating system	Scheduling management	5		L3

5. Content for Placement, Profession, HE and GATE

The content is not included in this course, but required to meet industry & profession requirements and help students for Placement, GATE, Higher Education, Entrepreneurship, etc. Identifying Area / Content requires experts consultation in the area.
Topics included are like, a. Advanced Topics, b. Recent Developments, c. Certificate Courses, d. Course Projects, e. New Software Tools, f. GATE Topics, g. NPTEL Videos, h. Swayam videos etc.

Modules	Topic / Description	Area	Remarks	Blooms Level

B. OBE PARAMETERS

1. Course Outcomes

Expected learning outcomes of the course, which will be mapped to POs.

Modules	Course Code.#	Course Outcome **At the end of the course, student should be able to . . .**	Teach. Hours	Instr Method	Assessment Method	Blooms' Level
1	17EC62.1	Describe the architectural features and instructions of 32 bit microcontroller ARM Cortex M3.	10	Lecture	Slip Test	L2 Understand
2	17EC62.2	Apply the knowledge gained for Programming ARM Cortex M3 for different applications.	10	Lecture	Assignment	L4
3	17EC62.3	Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.	10	Lecture	Assignment and Slip Test	L2 Understand
4	17EC62.4	Develop the hardware /software co-design and firmware design approaches.	10	Lecture and Tutorial	Assignment	L3 Apply
5	17EC62.5	Explain the need of real time operating system for embedded system applications.	10	Lecture	Slip test	L3 Apply
-	-	**Total**	**50**	-	-	-

2. Course Applications

Write 1 or 2 applications per CO.
Students should be able to employ / apply the course learnings to . . .

Modules	Application Area Compiled from Module Applications.	CO	Level
1	ARM processors are used in networking fields like home gateway, DSL modems for high speed internet communication and wireless communication.	CO1	L2
1	ARM processors are used in automotive industries.	CO1	L4
2	ARM processors are used in mobile and consumer devices.	CO2	L2
2	ARM processors are used in mass storage and imaging.	CO2	L3
3	Design Of Embedded Systems	CO3	L2
4	Design of ASIC.	CO4	L3
5	Design of any embedded system.	CO5	L3

3. Articulation Matrix

CO – PO Mapping with mapping level for each CO-PO pair, with course average attainment.

-	-	Course Outcomes	Program Outcomes														-
Modules	CO.#	**At the end of the course student should be able to . . .**	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3	Level
1	17EC62.1	Describe the architectural features and instructions of 32 bit microcontroller ARM Cortex M3.	3	3							2			1				
2	17EC62.2	Apply the knowledge gained for Programming ARM Cortex M3 for different applications.	3	3							2			1				
3	17EC62.3	Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.	3	3							2			1				
4	17EC62.4	Develop the hardware /software co-design and firmware design approaches.	3	3							2			1				
5	17EC62.5	Explain the need of real time operating system for embedded system applications.	3	3							2			1				
-	**17EC62.**	Average	**3**	**3**							**2**			**1**				**-**
-	*PO, PSO*	*1.Engineering Knowledge; 2.Problem Analysis; 3.Design / Development of Solutions; 4.Conduct Investigations of Complex Problems; 5.Modern Tool Usage; 6.The Engineer and Society; 7.Environment and Sustainability; 8.Ethics; 9.Individual and Teamwork; 10.Communication; 11.Project Management and Finance; 12.Life-long Learning; S1.Software Engineering; S2.Data Base Management; S3.Web Design*																

4. Curricular Gap and Content

Topics & contents not covered (from A.4), but essential for the course to address POs and PSOs.

Modules	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1	Keil	Seminar	3rd week of March 2020		List from B4 above
2	Keil programs for cortex m3	Seminar	3rd Week April 2020		List from B4 above

C. COURSE ASSESSMENT

1. Course Coverage

Assessment of learning outcomes for Internal and end semester evaluation.

Modules	Title	Teach. Hours	No. of question in Exam						CO	Levels
			CIA-1	CIA-2	CIA-3	Asg	Extra Asg	SEE		
1	ARM-32 bit Microcontroller.	10	2	-	-	1	1	2	CO1, CO2	L1, L2
2	ARM Cortex M3 Instruction Sets and Programming.	10	2	-	-	1	1	2	CO3, CO4	L2, L3
3	Embedded System Components.	10	-	2	-	1	1	2	CO5, CO6	L2, L3

4	Embedded System Design Concepts.	10	-	2	-	1	1	2	CO7, C08	L2, L3
5	RTOS and IDE for Embedded System Design.	10	-	-	4	1	1	2	CO9, CO10	L2, L3
-	**Total**	**50**	**4**	**4**	**4**	**5**	**5**	**10**	**-**	**-**

2. Continuous Internal Assessment (CIA)

Assessment of learning outcomes for Internal exams. Blooms Level in last column shall match with A.2.

Modules	Evaluation	Weightage in Marks	CO	Levels
1, 2	CIA Exam – 1	30	CO1,CO2	L1,L2, L3
3, 4	CIA Exam – 2	30	CO3,CO4	L2, L3
5	CIA Exam – 3	30	CO5	L2, L3
1, 2	Assignment - 1	10	CO1,CO2	L1,L2, L3
3, 4	Assignment - 2	10	CO3,CO4	L2, L3
5	Assignment - 3	10	CO5	L2, L3
1, 2	Seminar - 1		-	-
3, 4	Seminar - 2		-	-
5	Seminar - 3		-	-
1, 2	Quiz - 1		-	-
3, 4	Quiz - 2		-	-
5	Quiz - 3		-	-
1 - 5	Other Activities – Mini Project	-		
	Final CIA Marks		**-**	**-**

D1. TEACHING PLAN - 1

Module - 1

Title:		Appr Time:	10 Hrs
a	***Course Outcomes***	**CO**	**Blooms**
	Describe the architectural features and instructions of 32 bit microcontroller ARM Cortex M3.	CO1	**L2**
b	***Course Schedule***	-	-
Class No	**Portion covered per hour**	**-**	**-**
1	Thumb-2 technology and applications of ARM	CO1	L2
2	Architecture of ARM Cortex M3	CO1	L2
3	Various Units in the architecture	CO1	L2
4	Debugging support	CO1	L2
5	General Purpose Registers	CO1	L2
6	Special Registers	CO2	L2
7	exceptions	CO2	L2
8	interrupts	CO2	L2
9	stack operation	CO2	L2
10	reset sequence.	CO2	L2
c	**Application Areas**		
-	Students should be able employ / apply the Module learnings to . . .		
1	ARM processors are used in networking fields like home gateway, DSL modems for high speed internet communication and wireless communication.	CO1	L3

2	ARM processors are used in automotive industries.	CO1	L4
3	ARM processors are used in mobile and consumer devices.	CO1	L3
4	ARM processors are used in mass storage and imaging.	CO1	L4
d	**Review Questions**		
-			
1	Briefly describe the functions of the various units with the architectural block diagram of ARM Cortex M3.	CO1	L3
2	Explain the applications of Cortex M3.	CO1	L3
3	Discuss the functions of R0 to R15 and other special registers in Cortex M3.	CO1	L3
4	Describe the functions of exceptions with a vector table and priorities.	CO1	L3
5	Explain the operation modes of Cortex M3 with diagrams.	CO1	L3
6	Explain two stack model and reset sequence in ARM cortex M3.	CO1	L3
7	Explain the architecture of ARM Cortex-M3 processor with the help of a neat block diagram.	CO1	L3
8	List the applications of ARM Cortex-M3 processor	CO1	L3
9	Explain ARM Cortex-M3 Program Status Register in detail.	CO1	L3
10	Explain Stack PUSH and POP operation in Cortex-M3 with the help of a neat diagram.	CO1	L3
11	Explain reset sequence with the help of memory map.	CO1	L3
12	With a neat diagram explain the architecture of ARM cortex M3 micro controller.	CO1	L3
13	Explain the register organization of ARM cortex M3.	CO1	L3
14		CO1	L3
15	Explain the operation modes and privilege levels available in ARM cortex m3 with a neat transition diagram.	CO1	L3
16	Mention the instruction used for accessing the special registers. Explain the same using suitable examples.	CO1	L3
17	Explain the stack operation using push and pop instructions in the ARM cortex M3.	CO1	L3

Module – 2

Title:		Appr Time:	10 Hrs
a	***Course Outcomes***	**CO**	**Blooms**
-	Apply the knowledge gained for Programming ARM Cortex M3 for different applications.	CO2	**L3**
b	***Course Schedule***	-	-
Class No	**Portion covered per hour**	**-**	**-**
11	Assembly basics	CO3	L3
12	Instruction list and description	CO3	L3
13	Instruction list and description	CO3	L3
14	Useful instructions	CO3	L3
15	Memory mapping	CO3	L3
16	Bit-band operations and CMSIS	CO3	L3
17	Bit-band operations and CMSIS	CO4	L3
18	Assembly Programming	CO4	L3
19	Assembly and C language Programming	CO4	L3
20	C language Programming	CO4	L3
c	**Application Areas**	**-**	**-**
-	Students should be able employ / apply the Module learnings to . . .	-	-

1	ARM processors are used in networking fields like home gateway, DSL modems for high speed internet communication and wireless communication.	CO3	L3
2	ARM processors are used in automotive industries.	CO4	L3
3	ARM processors are used in mobile and consumer devices.	CO3	L3
4	ARM processors are used in mass storage and imaging.	CO4	L3
			L3
d	**Review Questions**	-	L3
-			L3
1	Explain the following 16 bit instructions in Cortex M3: ADC, RSB, TST, BL, LDR, MOV, SVC, PUSH	CO2	L3
2	Write an ALP to find the sum of first 10 integer numbers.	CO2	L3
3	Write the memory map of Cortex M3 and explain briefly bit-band operations.	CO2	L3
4		CO2	L3
5	Explain the following 32 bit instructions in Cortex M3: AND, CMN, MLA, SDIV, STR, MRS, MRS, POP.	CO2	L3
6	Write a C language program to toggle an LED with a small delay in Cortex M3.	CO2	L3
7	Explain the following instructions with example i)ASR ii)LSL iii)ROR iv)REV	CO2	L3
8	List and explain the function of any four data processing and branch instructions in Cortex- M3 with example.	CO2	L3
9	List and explain the function of any four commonly used memory access instructions in Cortex- M3.	CO2	L3
10	Write a note on the interface between assembly and C.	CO2	L3
11	Explain any two methods of accessing memory mapped registers in C.	CO2	L3
12	List and explain the function of any four commonly used memory access instructions in Cortex- M3.	CO2	L3
13	Explain shift and rotate instructions available in ARM cortex M3 instruction set. Why is there rotate right instruction but no rotate left instruction in ARM cortex M3.	CO2	L3
14	Explain the following with suitable examples. i) BFC ii) SXTH iii) UBFX iv) RBIT	CO2	L3
15	List and explain the function of any four commonly used memory access instructions in Cortex- M3.	CO2	L3
16	Write the memory map and explain memory access attributes in Cortex M3.	CO2	L3
17	Analyze the following instructions and write the contents of the register the execution of each instruction. Assume R8=0X00000088, R9=0X00000006,R10=0X00001111 i) RSB.W R8, R9, #0X10 ii) ADD R8, R9,R3 iii) BIC.W R6,R8 #0X06 iv) ORR R8,R9	CO2	L3

E1. CIA EXAM – 1

a. Model Question Paper - 1

Crs Code:	17EC62	Sem:	VI	Marks:	30	Time:	90 minutes
Course:	ARM Microcontroller & Embedded System						

-	-	**Note: Answer all questions, each carry equal marks. Module : 1, 2**	**Marks**	**CO**	**Level**
1	a	With a neat block diagram explain the simplified architecture of ARM controller.	8	CO2	L2
	b	What are the basic data processing instructions.	7	CO2	L2
2	a	Explain the evolution of ARM controller	8	CO1	L3
	b	What are the advantages of having NVIC	7	CO2	L2

3	a	List out the branching instructions of 16 bit and 32 bit in Cortex M3	8	CO3	L2
	b	What are the operation modes of Cortex M3. explain in detail	7	CO4	L3
4	a	Explain in detail Special registers in ARM Corter M3	8	CO3	L3
	b	What are all the debugging support present in ARM Cortex M3	7	CO4	L3

b. Assignment -1

Model Assignment Questions							
Crs Code:	17EC62	Sem:	VI	Marks:	30	Time:	90 minutes
Course:	ARM Microcontroller & Embedded System						

SNo	Assignment Description	Marks	CO	Level
1	Briefly describe the functions of the various units with the architectural block diagram of ARM Cortex M3.	7	CO1	L3
2	Explain the applications of Cortex M3.	8	CO1	L3
3	Discuss the functions of R0 to R15 and other special registers in Cortex M3.	7	CO1	L3
4	Describe the functions of exceptions with a vector table and priorities.	8	CO1	L3
5	Explain the operation modes of Cortex M3 with diagrams.	7	CO1	L3
6	Explain two stack model and reset sequence in ARM cortex M3.	8	CO1	L3
7	Explain the architecture of ARM Cortex-M3 processor with the help of a neat block diagram.	7	CO1	L3
8	List the applications of ARM Cortex-M3 processor	8	CO1	L3
9	Explain ARM Cortex-M3 Program Status Register in detail.	7	CO1	L3
10	Explain Stack PUSH and POP operation in Cortex-M3 with the help of a neat diagram.	8	CO1	L3
11	Explain reset sequence with the help of memory map.	7	CO1	L3
12	With a neat diagram explain the architecture of ARM cortex M3 micro controller.	8	CO1	L3
13	Explain the register organization of ARM cortex M3.	7	CO1	L3
14	Explain the following 32 bit instructions in Cortex M3: AND, CMN, MLA, SDIV, STR, MRS, MRS, POP.	8	CO2	L3
15	Explain the operation modes and privilege levels available in ARM cortex m3 with a neat transition diagram.	7	CO2	L3
16	Mention the instruction used for accessing the special registers. Explain the same using suitable examples.	8	CO2	L3
17	Explain the stack operation using push and pop instructions in the ARM cortex M3.	7	CO2	L3
18	Explain the following 16 bit instructions in Cortex M3: ADC, RSB, TST, BL, LDR, MOV, SVC, PUSH	8	CO2	L3
19	Write an ALP to find the sum of first 10 integer numbers.	7	CO2	L4
20	Write the memory map of Cortex M3 and explain briefly bit-band operations.	8	CO2	L4
21	Explain the following 32 bit instructions in Cortex M3: AND, CMN, MLA, SDIV, STR, MRS, MRS, POP.	7	CO2	L3

22	Explain the following 32 bit instructions in Cortex M3: AND, CMN, MLA, SDIV, STR, MRS, MRS, POP.	8	CO2	L3
23	Write a C language program to toggle an LED with a small delay in Cortex M3.	7	CO2	L3
24	Explain the following instructions with example i)ASR ii)LSL iii)ROR iv)REV	8	CO2	L3
25	List and explain the function of any four data processing and branch instructions in Cortex- M3 with example.	7	CO2	L3
26		8	CO2	L3
27	Write a note on the interface between assembly and C.	7	CO2	L3
28	Explain any two methods of accessing memory mapped registers in C.	8	CO2	L3
29	List and explain the function of any four commonly used memory access instructions in Cortex- M3.	7	CO2	L3
30	Explain shift and rotate instructions available in ARM cortex M3 instruction set. Why is there rotate right instruction but no rotate left instruction in ARM cortex M3.	8	CO2	L3
31	Explain the following with suitable examples. i) BFC ii) SXTH iii) UBFX iv) RBIT	7	CO2	L3
32		8	CO2	L3
33	Write the memory map and explain memory access attributes in Cortex M3.	7	CO2	L3
34	Analyze the following instructions and write the contents of the register the execution of each instruction. Assume R8=0X00000088, R9=0X00000006,R10=0X00001111 i) RSB.W R8, R9, #0X10 ii) ADD R8, R9,R3 iii) BIC.W R6,R8 #0X06 iv) ORR R8,R9	8	CO2	L3
35	Explain Stack PUSH and POP operation in Cortex-M3 with the help of a neat diagram.	7	CO2	L3
36	Explain reset sequence with the help of memory map.	8	CO2	L3
37	With a neat diagram explain the architecture of ARM cortex M3 micro controller.	7	CO2	L3
38	Explain the register organization of ARM cortex M3.	8	CO2	L3
39	Explain the following 32 bit instructions in Cortex M3: AND, CMN, MLA, SDIV, STR, MRS, MRS, POP.	7	CO2	L3
40	Explain the operation modes and privilege levels available in ARM cortex m3 with a neat transition diagram.	8	CO2	L3
41	Mention the instruction used for accessing the special registers. Explain the same using suitable examples.	7	CO2	L3
42	Explain the stack operation using push and pop instructions in the ARM cortex M3.	8	CO2	L3
43	Explain the following 16 bit instructions in Cortex M3: ADC, RSB, TST, BL, LDR, MOV, SVC, PUSH	7	CO2	L3
44	Write an ALP to find the sum of first 10 integer numbers.	8	CO2	L4
45	Write the memory map of Cortex M3 and explain briefly bit-band operations.	7	CO2	L4
46	Explain the following instructions with example i)ASR ii)LSL iii)ROR iv)REV	8	CO2	L3
47	Explain the following 32 bit instructions in Cortex M3: AND, CMN, MLA, SDIV, STR, MRS, MRS, POP.	7	CO2	L3
48	Write a C language program to toggle an LED with a small delay in Cortex M3.	8	CO2	L3
49	Explain the following instructions with example i)ASR ii)LSL iii)ROR iv)REV	7	CO2	CO3
50	List and explain the function of any four data processing and branch instructions in Cortex- M3 with example.	8	CO2	CO4

D2. TEACHING PLAN - 2

Module – 3

Title:		Appr Time:	10 Hrs
a	***Course Outcomes***	**CO**	**Blooms**
-	At the end of the topic the student should be able to . . .	-	**Level**
	Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.	CO3	L2
b	***Course Schedule***		
Class No	**Portion covered per hour**	**-**	**-**
21	**Embedded System Components:** Embedded Vs General computing system,	CO3	L2
22	Classification of Embedded systems,	CO3	L2
23	Major applications and purpose of ES.	CO3	L2
24	Core of an Embedded System including all types of processor/controller,	CO3	L2
25	Memory, Sensors,	CO3	L2
26	Actuators, LED, 7 segment LED display,	CO3	L2
27	Optocoupler, Relay,	CO3	L2
28	Push button switch, Piezo buzzer,	CO3	L2
29	Communication Interface (onboard and external types),	CO3	L2
30	Embedded firmware, Other system components.	CO3	L2
c	**Application Areas**	**-**	**-**
-	Students should be able employ / apply the Module learnings to . . .	-	-
1	Design Of Embedded Systems	CO3	L2
d	**Review Questions**	-	-
-	The attainment of the module learning assessed through following questions	-	-
1	Explain the components of a typical embedded system in detail.	CO3	L2
2	Which are the components used as the core of an embedded system? Explain the merits, drawbacks, if any.	CO3	L2
3	What is the difference between Application Specific Integrated Circuit (ASIC) Application Specific Standard Product (ASSP).	CO3	L2
4	Explain the 6 purposes of Embedded systems with an example for each.	CO3	L2
5	Differentiate between (i) General Computing Systems and Embedded Systems (ii) RISC and CISC architectures.	CO3	L2
6	Explain the 3 classifications of Embedded systems based on complexity and performance.	CO3	L2
7	Mention the applications of Embedded systems with an example for each.	CO3	L2
8	Explain the functions of Optocoupler and SPI bus with diagrams.	CO3	L2
9	Write a note on Embedded firmware.	CO3	L2
10	Explain SRAM design and features with a diagram.	CO3	L2
11	Write the architectural block diagram of embedded system and mention the components used.	CO3	L2
12	Explain the components of typical Embedded Systems in detail.	CO3	L2
13	Give the memory classification. Explain the SRAM cell implementation with relevant figures.	CO3	L2
14	Explain the different on-board communication interfaces in brief.	CO3	L2
15	Differentiate between computer system and an Embedded System.	CO3	L2
16	Differentiate the following i) RISC and SISC architecture. ii) Little endian and Big endian architecture.	CO3	L2

17	What are the features of the following I) I²C Bus ii) IrDA iii) Optocoupler iv) 1-wire interface	CO3	L2
18	What are the different memories types memories used in embedded system design. Explain the role of each.	CO3	L2
19	Explain the following circuits in an embedded system: I) brown out protection circuits ii) reset circuit	CO3	L2

Module – 4

Title:	Data Transmission and Telemetry Measurement of Non – Electrical Quantities	Appr Time:	10 Hrs
a	***Course Outcomes***	**CO**	**Blooms**
-	At the end of the topic the student should be able to . . .	-	**Level**
	Develop the hardware /software co-design and firmware design approaches	CO4	L3
b	***Course Schedule***		
Class No	**Portion covered per hour**	**-**	**-**
31	**Embedded System Design Concepts:** Characteristics of Embedded Systems,	CO4	L3
32	Characteristics and Quality Attributes of Embedded Systems,	CO4	L3
33	Operational and non-operational quality attributes,	CO4	L3
34	Operational and non-operational quality attributes,	CO4	L3
35	Embedded 86 Systems-Application and Domain specific,	CO4	L3
36	Embedded 86 Systems-Application and Domain specific,	CO4	L3
37	Hardware Software Co-Design and Program Modelling (excluding UML),	CO4	L3
38	Hardware Software Co-Design and Program Modelling (excluding UML),	CO4	L3
39	Embedded firmware design and development (excluding C language).	CO4	L3
40	Embedded firmware design and development (excluding C language).	CO4	L3
c	**Application Areas**	**-**	**-**
-	Students should be able employ / apply the Module learnings to . . .	-	-
1	Design of ASIC.	CO4	L3
2	Design of any embedded system.	CO4	L4
d	**Review Questions**	-	-
-	The attainment of the module learning assessed through following questions	-	-
1	Define the 6 characteristics of an embedded system.	CO4	L3
2	Explain the 6 operational quality attributes of an embedded systems.	CO4	L3
3	With a block diagram, mention the components used in the design of a washing machine and also explain its working.	CO4	L3
4	Compare DFG and CDFG with an example and diagrams.	CO4	L3
5	With FSM model, explain the design and operation of automatic tea/ coffee vending machine.	CO4	L3
6	Explain the assembly language based embedded firmware development with a diagram and mention its advantages and disadvantages.	CO4	L3
7	Explain the different characteristics of Embedded System in detail.	CO4	L3
8	What is operational quality attribute? Explain the important non- operational quality attributes to be considered in any Embedded System design.	CO4	L3
9	Explain the different Embedded firmware design approaches in detail.	CO4	L3
10	What is Hardware and Software co-design? Explain the fundamental design approaches in detail.	CO4	L3
11	Explain the term quality attributes in embedded system development context. What are the different quality attributes to be considered in an embedded	CO4	L3

	system design.		
12	Explain the data flow graph and control flow graph models in the embedded system.	CO4	L3
13		CO4	L3
14	Explain the different embedded firmware design approach in detail.	CO4	L3
15	Explain the characteristics pf embedded system.	CO4	L3
e	**Experiences**	-	-
1		CO7	L2
2			

E2. CIA EXAM – 2

a. Model Question Paper - 2

Crs Code:	17EC62	Sem:	VI	Marks:	30	Time	90 minutes
Course:	ARM Microcontroller and Embedded Systems						

-	-	**Note: Answer all questions, each carry equal marks. Module : 3, 4**	**Marks**	**CO**	**Level**
1	a	Explain briefly signed saturation operation	8	CO3	L1
	b	With a neat diagram explain the predefined memory map in cortex M3	7	CO3	L2
2	a	Write short notes on any two i) Flag bits ii) TBB and TBH iii)Reverse operations	8	CO3	L2
	b	In detail explain the bit band operations	7	CO3	L4
3	a	Classify embedded systems in detail and explain them.	8	CO4	L2
	b	Define Embedded Systems and differentiate embedded systems with general computing systems	7	CO4	L2
4	a	Write short notes on any two i) Endian mode ii) Applications of embedded systems iii)Exclusive access	8	CO4	L3
	b	Explain the arm development tools in detail.	7	CO4	L3

b. Assignment – 2

Model Assignment Questions							
Crs Code:		Sem:		Marks:		Time:	
Course:							

SNo	Assignment Description	Marks	CO	Level
1	Explain the components of a typical embedded system in detail.	7	CO3	L2
2	Which are the components used as the core of an embedded System? Explain the merits, drawbacks, if any.	8	CO3	L2
3	What is the difference between Application Specific Integrated Circuit (ASIC) Application Specific Standard Product (ASSP).	7	CO3	L2
4	Explain the 6 purposes of Embedded systems with an example for each.	8	CO3	L2
5	Differentiate between (i) General Computing Systems and Embedded Systems (ii) RISC and CISC architectures.	7	CO3	L2
6	Explain the 3 classifications of Embedded systems based on	8	CO3	L2

	complexity and performance.			
7	Mention the applications of Embedded systems with an example for each.	5	CO3	L2
8	Explain the functions of Optocoupler and SPI bus with diagrams.	6	CO3	L2
9	Write a note on Embedded firmware.	7	CO3	L2
10	Explain SRAM design and features with a diagram.	8	CO3	L2
11	Write the architectural block diagram of embedded system and mention the components used.	7	CO3	L2
12	Explain the components of typical Embedded Systems in detail.	8	CO3	L2
13	Give the memory classification. Explain the SRAM cell implementation with relevant figures.	7	CO3	L2
14	Explain the different on-board communication interfaces in brief.	8	CO3	L2
15	Differentiate between computer system and an Embedded System.	7	CO3	L2
16	Differentiate the following i) RISC and SISC architecture. ii) Little endian and Big endian architecture.	8	CO3	L2
17	What are the features of the following I) I^2C Bus ii) IrDA iii) Optocoupler iv) 1-wire interface	7	CO3	L2
18	What are the different memories types memories used in embedded system design. Explain the role of each.	8	CO3	L2
19	Explain the following circuits in an embedded system: I) brown out protection circuits ii) reset circuit	7	CO3	L2
20	Define the 6 characteristics of an embedded system.	8	CO3	L2
21	Explain the 6 operational quality attributes of an embedded systems.	7	CO4	L3
22	With a block diagram, mention the components used in the design of a washing machine and also explain its working.	8	CO4	L3
23	Compare DFG and CDFG with an example and diagrams.	7	CO4	L3
24	With FSM model, explain the design and operation of automatic tea/ coffee vending machine.	8	CO4	L3
25	Explain the assembly language based embedded firmware development with a diagram and mention its advantages and disadvantages.	7	CO4	L3
26	Explain the different characteristics of Embedded System in detail.	8	CO4	L3
27	What is operational quality attribute? Explain the important non- operational quality attributes to be considered in any Embedded System design.	7	CO4	L3
28	Explain the different Embedded firmware design approaches in detail.	8	CO4	L3
29	What is Hardware and Software co-design? Explain the fundamental design approaches in detail.	7	CO4	L3
30	Explain the term quality attributes in embedded system development context. What are the different quality attributes to be considered in an embedded system design.	8	CO4	L3
31	Explain the data flow graph and control flow graph models in the embedded system.	7	CO4	L3
32		8	CO4	L3
33	Explain the different embedded firmware design approach in	7	CO4	L3

	detail.			
34	Explain the components of a typical embedded system in detail.	8	CO4	L3
35	Which are the components used as the core of an embedded system? Explain the merits, drawbacks, if any.	7	CO4	L3
36	What is the difference between Application Specific Integrated Circuit (ASIC) Application Specific Standard Product (ASSP).	8	CO4	L3
37	Explain the 6 purposes of Embedded systems with an example for each.	7	CO4	L3
38	Differentiate between (i) General Computing Systems and Embedded Systems (ii) RISC and CISC architectures.	8	CO4	L3
39	Explain the 3 classifications of Embedded systems based on complexity and performance.	7	CO4	L3
40	Mention the applications of Embedded systems with an example for each.	8	CO4	L3
41	Explain the functions of Optocoupler and SPI bus with diagrams.	7	CO4	L3
42	Write a note on Embedded firmware.	8	CO4	L3
43	Explain SRAM design and features with a diagram.	7	CO4	L3
44	Write the architectural block diagram of embedded system and mention the components used.	8	CO4	L3
45	Explain the components of typical Embedded Systems in detail.	7	CO4	L3
46	Give the memory classification. Explain the SRAM cell implementation with relevant figures.	8	CO4	L3
47	Explain the different on-board communication interfaces in brief.	7	CO4	L3
48	Differentiate between computer system and an Embedded System.	8	CO4	L3
49	Differentiate the following i) RISC and SISC architecture. ii) Little endian and Big endian architecture.	7	CO4	L3
50	What are the features of the following I) I^2C Bus ii) IrDA iii) Optocoupler iv) 1-wire interface	8	CO4	L3
51	What are the different memories types memories used in embedded system design. Explain the role of each.	7	CO4	L3
52	Explain the following circuits in an embedded system: I) brown out protection circuits ii) reset circuit	8	CO4	L3
53	Define the 6 characteristics of an embedded system.	7	CO4	L3
54	Explain the 6 operational quality attributes of an embedded systems.	8	CO4	L3
55	With a block diagram, mention the components used in the design of a washing machine and also explain its working.	7	CO4	L3
56	Compare DFG and CDFG with an example and diagrams.	8	CO4	L3
57	With FSM model, explain the design and operation of automatic tea/ coffee vending machine.	7	CO4	L3
58	Explain the assembly language based embedded firmware development with a diagram and mention its advantages and disadvantages.	8	CO4	L3
59	Explain the components of a typical embedded system in detail.	7	CO4	L3

60	Which are the components used as the core of an embedded system? Explain the merits, drawbacks, if any.	8	CO4	L3
61	What is the difference between Application Specific Integrated Circuit (ASIC) Application Specific Standard Product (ASSP).	7	CO4	L3
62	Explain the 6 purposes of Embedded systems with an example for each.	8	CO4	L3

D3. TEACHING PLAN - 3

Module – 5

Title:	Loop and Horn Antenna and Antenna Types	Appr Time:	10 Hrs
a	***Course Outcomes***	**CO**	**Blooms**
-	At the end of the topic the student should be able to . . .	-	**Level**
	Explain the need of real time operating system for embedded system applications.		L3
b	***Course Schedule***	-	-
Class No	**Portion covered per hour**	**-**	**-**
41	**RTOS and IDE for Embedded System Design:** Operating System basics,	CO5	L3
42	Types of operating systems,	CO5	L3
43	Task, process and threads (Only POSIX Threads with an example program),	CO5	L3
44	Thread preemption, Preemptive Task scheduling techniques,	CO5	L3
45	Task Communication,	CO5	L3
46	Task synchronization issues – Racing and Deadlock,	CO5	L3
47	Concept of Binary and counting semaphores (Mutex example without any program),	CO5	L3
48	How to choose an RTOS, Integration and testing of Embedded hardware and firmware	CO5	L3
49	Integration and testing of Embedded hardware and firmware,	CO5	L35
50	Embedded system Development Environment – Block diagram (excluding Keil), Disassembler/decompiler, simulator, emulator and debugging techniques	CO5	L3
c	**Application Areas**	**-**	**-**
-	Students should be able employ / apply the Module learnings to . . .	-	-
1	Design of ASIC.	CO5	L3
2	Design of any embedded system with RTOS.	CO5	L4
d	**Review Questions**	-	-
-	The attainment of the module learning assessed through following questions	-	-
1	Explain the concept of deadlock with a block diagram. Mention the different conditions which favours a deadlock condition.	CO5	L1
2	Write a block diagram of IDE environment for an embedded system design explain their function in brief.	CO5	L3
3	Three processes with process IDs P1,P2,P3 with estimated completion time 10,5,7 ms respectively enters the ready queue together. A new process P4 with completion time 2 ms enters the ready queue after 2ms. Calculate the waiting time for all the processes. Also calculate the average waiting time and average turn around time . The algorithm used is SJF based preemptive scheduling. Assume all the processes contain only CPU operation and no I/O operation involved.	CO5	L2
4	Mention the sequence of operations for embedding the firmware with a programmer and draw the interfacing diagram.	CO5	L3

5	Briefly explain the functions of the operating system, with a diagram.	CO5	L3
6	Describe preemptive SJF scheduling. Determine average turn around time and average waiting time, if processes P1 P2 and P3 with estimated completion time of 10, 5, 7 milliseconds enter ready queue together and later P4 with a completion time of 2 msec enters ready queue after 2 msec.	CO5	L4
7	With a state transition diagram, structure and memory organization of a process, describe the process state transitions.	CO5	L3
8	Explain out of circuit and in-system programming methods for integration of hardware and firmware.	CO5	L3
9	With a diagram, mention the function of the components in an embedded system development environment.	CO5	L3
10	Explain simulator based debugging and ICE based target debugging techniques.	CO5	L3
11	Explain the concept of deadlock with a block diagram. Mention the different conditions which favours a deadlock condition.	CO5	L3
12	Write a block diagram of IDE environment for an embedded system design explain their function in brief.	CO5	L3
13	Three processes with process IDs P1,P2,P3 with estimated completion time 10,5,7 ms respectively enters the ready queue together. A new process P4 with completion time 2 ms enters the ready queue after 2ms. Calculate the waiting time for all the processes. Also calculate the average waiting time and average turn around time . The algorithm used is SJF based preemptive scheduling. Assume all the processes contain only CPU operation and no I/O operation involved.	CO5	L3
14	Mention the sequence of operations for embedding the firmware with a programmer and draw the interfacing diagram.	CO5	L3
e	**Experiences**	-	-
1		CO10	L2
2		CO9	

E3. CIA EXAM – 3

a. Model Question Paper - 3

Crs Code:	17EC62	Sem:	VI	Marks:	30	Time:	75 minutes

Course: ARM Microcontroller and Embedded Systems

-	-	**Note: Answer any 2 questions, each carry equal marks.**	**Marks**	**CO**	**Level**
1	a	What are the other system components. Explain them	8	CO5	L1
	b	What are the types of communi8cation interface? brief them	7	CO5	L2
2	a	Write short notes on any two i) Relay ii) 7 Segment LED display	8	CO5	L2
	b	Briefly explain the types of Memory	7	CO5	L4
3	a	What are the quality attributes of ES.	8	CO5	L1
	b	What are the computational models. explain a simple warning system for seat belt using FSM	7	CO5	L2
4	a	Briefly explain the issues in hardware and software co-design	8	CO5	L2
	b	Explain the application specific ES taking washing machine as an example.	7	CO5	L2

b. Assignment – 3

Model Assignment Questions

Crs Code:		Sem:		Marks:		Time:	
Course:							

SNo	Assignment Description	Marks	CO	Level
1	Explain the concept of deadlock with a block diagram. Mention the different conditions which favours a deadlock condition.	7	CO5	L3
2	Write a block diagram of IDE environment for an embedded system design explain their function in brief.	8	CO5	L3
3	Three processes with process IDs P1,P2,P3 with estimated completion time 10,5,7 ms respectively enters the ready queue together. A new process P4 with completion time 2 ms enters the ready queue after 2ms. Calculate the waiting time for all the processes. Also calculate the average waiting time and average turn around time . The algorithm used is SJF based preemptive scheduling. Assume all the processes contain only CPU operation and no I/O operation involved.	7	CO5	L3
4	Mention the sequence of operations for embedding the firmware with a programmer and draw the interfacing diagram.	8	CO5	L3
5	Briefly explain the functions of the operating system, with a diagram.	5	CO5	L3
6	Describe preemptive SJF scheduling. Determine average turn around time and average waiting time, if processes P1 P2 and P3 with estimated completion time of 10, 5, 7 milliseconds enter ready queue together and later P4 with a completion time of 2 msec enters ready queue after 2 msec.	6	CO5	L3
7	With a state transition diagram, structure and memory organization of a process, describe the process state transitions.	7	CO5	L3
8	Explain out of circuit and in-system programming methods for integration of hardware and firmware.	8	CO5	L3
9	With a diagram, mention the function of the components in an embedded system development environment.	7	CO5	L3
10	Explain simulator based debugging and ICE based target debugging techniques.	8	CO5	L3
11	Explain the concept of deadlock with a block diagram. Mention the different conditions which favours a deadlock condition.	7	CO5	L3
12	Write a block diagram of IDE environment for an embedded system design explain their function in brief.	8	CO5	L3
13	Three processes with process IDs P1,P2,P3 with estimated completion time 10,5,7 ms respectively enters the ready queue together. A new process P4 with completion time 2 ms enters the ready queue after 2ms. Calculate the waiting time for all the processes. Also calculate the average waiting time and average turn around time . The algorithm used is SJF based preemptive scheduling. Assume all the processes contain only CPU operation and no I/O operation involved.	5	CO5	L3
14	Mention the sequence of operations for embedding the firmware with a programmer and draw the interfacing diagram.	6	CO5	L3
15	Explain the concept of deadlock with a block diagram. Mention the different conditions which favours a deadlock condition.	7	CO5	L3
16	Write a block diagram of IDE environment for an embedded system design explain their function in brief.	8	CO5	L3
17	Three processes with process IDs P1,P2,P3 with estimated completion time 10,5,7 ms respectively enters the ready queue together. A new process P4 with completion time 2 ms enters the ready queue after 2ms. Calculate the waiting time for all the processes. Also calculate the average waiting time and average turn around time . The algorithm used is SJF based preemptive scheduling. Assume all the processes contain only CPU operation and no I/O operation involved.	7	CO5	L3
18	Mention the sequence of operations for embedding the firmware with a programmer and draw the interfacing diagram.	8	CO5	L3

19	Briefly explain the functions of the operating system, with a diagram.	7	CO5	L3
20	Describe preemptive SJF scheduling. Determine average turn around time and average waiting time, if processes P1 P2 and P3 with estimated completion time of 10, 5, 7 milliseconds enter ready queue together and later P4 with a completion time of 2 msec enters ready queue after 2 msec.	8	CO5	L3
21	With a state transition diagram, structure and memory organization of a process, describe the process state transitions.	5	CO5	L3
22	Explain out of circuit and in-system programming methods for integration of hardware and firmware.	6	CO5	L3
23	With a diagram, mention the function of the components in an embedded system development environment.	7	CO5	L3
24	Explain simulator based debugging and ICE based target debugging techniques.	8	CO5	L3
25	Explain the concept of deadlock with a block diagram. Mention the different conditions which favours a deadlock condition.	7	CO5	L3
26	Write a block diagram of IDE environment for an embedded system design explain their function in brief.	8	CO5	L3
27	Three processes with process IDs P1,P2,P3 with estimated completion time 10,5,7 ms respectively enters the ready queue together. A new process P4 with completion time 2 ms enters the ready queue after 2ms. Calculate the waiting time for all the processes. Also calculate the average waiting time and average turn around time . The algorithm used is SJF based preemptive scheduling. Assume all the processes contain only CPU operation and no I/O operation involved.	7	CO5	L3
28	Mention the sequence of operations for embedding the firmware with a programmer and draw the interfacing diagram.	8	CO5	L3
29	Explain the concept of deadlock with a block diagram. Mention the different conditions which favours a deadlock condition.	5	CO5	L3
30	Write a block diagram of IDE environment for an embedded system design explain their function in brief.	6	CO5	L3
31	Three processes with process IDs P1,P2,P3 with estimated completion time 10,5,7 ms respectively enters the ready queue together. A new process P4 with completion time 2 ms enters the ready queue after 2ms. Calculate the waiting time for all the processes. Also calculate the average waiting time and average turn around time . The algorithm used is SJF based preemptive scheduling. Assume all the processes contain only CPU operation and no I/O operation involved.	7	CO5	L3
32	Mention the sequence of operations for embedding the firmware with a programmer and draw the interfacing diagram.	8	CO5	L3
33	Briefly explain the functions of the operating system, with a diagram.	7	CO5	L3
34	Describe preemptive SJF scheduling. Determine average turn around time and average waiting time, if processes P1 P2 and P3 with estimated completion time of 10, 5, 7 milliseconds enter ready queue together and later P4 with a completion time of 2 msec enters ready queue after 2 msec.	8	CO5	L3
35	With a state transition diagram, structure and memory organization of a process, describe the process state transitions.	7	CO5	L3
36	Explain out of circuit and in-system programming methods for integration of hardware and firmware.	8	CO5	L3
37	With a diagram, mention the function of the components in an embedded system development environment.	5	CO5	L3
38	Explain simulator based debugging and ICE based target debugging techniques.	6	CO5	L3
39	Explain the concept of deadlock with a block diagram. Mention the different conditions which favours a deadlock condition.	7	CO5	L3
40	Write a block diagram of IDE environment for an embedded system design explain their function in brief.	8	CO5	L3

41	Three processes with process IDs P1,P2,P3 with estimated completion time 10,5,7 ms respectively enters the ready queue together. A new process P4 with completion time 2 ms enters the ready queue after 2ms. Calculate the waiting time for all the processes. Also calculate the average waiting time and average turn around time . The algorithm used is SJF based preemptive scheduling. Assume all the processes contain only CPU operation and no I/O operation involved.	7	CO5	L3
42	Mention the sequence of operations for embedding the firmware with a programmer and draw the interfacing diagram.	8	CO5	L3
43	Explain the concept of deadlock with a block diagram. Mention the different conditions which favours a deadlock condition.	7	CO5	L3
44	Write a block diagram of IDE environment for an embedded system design explain their function in brief.	8	CO5	L3
45	Three processes with process IDs P1,P2,P3 with estimated completion time 10,5,7 ms respectively enters the ready queue together. A new process P4 with completion time 2 ms enters the ready queue after 2ms. Calculate the waiting time for all the processes. Also calculate the average waiting time and average turn around time . The algorithm used is SJF based preemptive scheduling. Assume all the processes contain only CPU operation and no I/O operation involved.	5	CO5	L3
46	Mention the sequence of operations for embedding the firmware with a programmer and draw the interfacing diagram.	6	CO5	L3
47	Briefly explain the functions of the operating system, with a diagram.	7	CO5	L3
48	Describe preemptive SJF scheduling. Determine average turn around time and average waiting time, if processes P1 P2 and P3 with estimated completion time of 10, 5, 7 milliseconds enter ready queue together and later P4 with a completion time of 2 msec enters ready queue after 2 msec.	8	CO5	L3
49	With a state transition diagram, structure and memory organization of a process, describe the process state transitions.	7	CO5	L3
50	Explain out of circuit and in-system programming methods for integration of hardware and firmware.	8	CO5	L3
51	With a diagram, mention the function of the components in an embedded system development environment.	7	CO5	L3
52	Explain simulator based debugging and ICE based target debugging techniques.	8	CO5	L3
53	Explain the concept of deadlock with a block diagram. Mention the different conditions which favours a deadlock condition.	5	CO5	L3
54	Write a block diagram of IDE environment for an embedded system design explain their function in brief.	6	CO5	L3
55	Three processes with process IDs P1,P2,P3 with estimated completion time 10,5,7 ms respectively enters the ready queue together. A new process P4 with completion time 2 ms enters the ready queue after 2ms. Calculate the waiting time for all the processes. Also calculate the average waiting time and average turn around time . The algorithm used is SJF based preemptive scheduling. Assume all the processes contain only CPU operation and no I/O operation involved.	7	CO5	L3
56	Mention the sequence of operations for embedding the firmware with a programmer and draw the interfacing diagram.	8	CO5	L3
57	Explain the concept of deadlock with a block diagram. Mention the different conditions which favours a deadlock condition.	7	CO5	L3
58	Write a block diagram of IDE environment for an embedded system design explain their function in brief.	8	CO5	L3
59	Three processes with process IDs P1,P2,P3 with estimated completion time 10,5,7 ms respectively enters the ready queue together. A new process P4 with completion time 2 ms enters the ready queue after 2ms. Calculate the waiting time for all the processes. Also calculate the average waiting time and average turn around time . The algorithm used is SJF based preemptive scheduling. Assume all the processes	7	CO5	L3

	contain only CPU operation and no I/O operation involved.			
60	Mention the sequence of operations for embedding the firmware with a programmer and draw the interfacing diagram.	8	CO5	L3
61	Briefly explain the functions of the operating system, with a diagram.	5	CO5	L3
62	Describe preemptive SJF scheduling. Determine average turn around time and average waiting time, if processes P1 P2 and P3 with estimated completion time of 10, 5, 7 milliseconds enter ready queue together and later P4 with a completion time of 2 msec enters ready queue after 2 msec.	6	CO5	L3

F. EXAM PREPARATION

1. University Model Question Paper

Course:	ARM Microcontroller and Embedded Systems							
Crs Code:	17EC62	Sem:	6	Marks:	60			
-	**Note**	Answer all FIVE full questions. All questions carry equal marks.						**Marks**
1	a	Briefly describe the functions of the various units with the architectural block diagram of ARM Cortex M3.				CO1	L2	6
	b	Explain the applications of Cortex M3.				CO1	L3	3
	c	Discuss the functions of R0 to R15 and other special registers in Cortex M3.				CO1	L3	7
2	a	Describe the functions of exceptions with a vector table and priorities.				CO1	L3	6
	b	Explain the operation modes of Cortex M3 with diagrams.				CO1	L3	3
	c	Explain two stack model and reset sequence in ARM cortex M3.				CO1	L3	7
3	a	Explain the following 16 bit instructions in Cortex M3: ADC, RSB, TST, BL, LDR, MOV, SVC, PUSH				CO2	L3	7
	b	Write an ALP to find the sum of first 10 integer numbers.				CO2	L4	4
	c	Write the memory map of Cortex M3 and explain briefly bit-band operations.				CO2	L4	5
4	a	Explain the following 32 bit instructions in Cortex M3: AND, CMN, MLA, SDIV, STR, MRS, MRS, POP.				CO2	L3	8
	b	Write a C language program to toggle an LED with a small delay in Cortex M3.				CO2	L3	4
	c	With a diagram, explain the organization of CMSIS.				CO2	L3	4
5	a	Explain the 6 purposes of Embedded systems with an example for each.				CO3	L3	6
	b	Differentiate between (i) General Computing Systems and Embedded Systems (ii) RISC and CISC architectures.				CO3	L3	4
	c	Explain the 3 classifications of Embedded systems based on complexity and performance.				CO3	L3	3
	d	Mention the applications of Embedded systems with an example for each.				CO3	L3	3
6	a	Explain the functions of Optocoupler and SPI bus with diagrams.				CO3	L3	6
	b	Write a note on Embedded firmware.				CO3	L3	4
	c	Explain SRAM design and features with a diagram.				CO3	L3	3
	d	Write the architectural block diagram of embedded system and mention the components used.				CO3	L3	3

7	a	Define the 6 characteristics of an embedded system.	CO4	L3	5
	b	Explain the 6 operational quality attributes of an embedded systems.	CO4	L3	5
	c	With a block diagram, mention the components used in the design of a washing machine and also explain its working.	CO4	L3	6
8	a	Compare DFG and CDFG with an example and diagrams.	CO4	L3	4
	b	With FSM model, explain the design and operation of automatic tea/ coffee vending machine.	CO4	L3	5
	c	Explain the assembly language based embedded firmware development with a diagram and mention its advantages and disadvantages.	CO4	L3	7
9	a	Briefly explain the functions of the operating system, with a diagram.	CO5	L3	4
	b	Describe preemptive SJF scheduling. Determine average turn around time and average waiting time, if processes P1 P2 and P3 with estimated completion time of 10, 5, 7 milliseconds enter ready queue together and later P4 with a completion time of 2 msec enters ready queue after 2 msec.	CO5	L3	5
	c	With a state transition diagram, structure and memory organization of a process, describe the process state transitions.	CO5	L3	7
10	a	Explain out of circuit and in-system programming methods for integration of hardware and firmware.	CO5	L3	5
	b	With a diagram, mention the function of the components in an embedded system development environment.	CO5	L3	5
	c	Explain simulator based debugging and ICE based target debugging techniques.	CO5	L3	6

2. SEE Important Questions

Course:		ARM Microcontroller and Embedded Systems						Month / Year		May /2018	
Crs Code:		17EC62	Sem:	6	Marks:	80		Time:		180 minutes	
	Note	Answer all FIVE full questions. All questions carry equal marks.						-		-	
Module	Qno.	Important Question						**Marks**		**CO**	**Year**
1	a	With a neat diagram explain the architecture of ARM cortex M3 micro controller.						10		CO1	2018
	b	Explain the register organization of ARM cortex M3.						6		CO1	2018
2	a	Explain the operation modes and privilege levels available in ARM cortex m3 with a neat transition diagram.						6		CO1	2018
	b	Mention the instruction used for accessing the special registers. Explain the same using suitable examples.						4		CO1	2018
	c	Explain the stack operation using push and pop instructions in the ARM cortex M3.						6		CO1	2018
3	a	Explain shift and rotate instructions available in ARM cortex M3 instruction set. Why is there rotate right instruction but no rotate left instruction in ARM cortex M3.						8		CO2	2018
	b	Explain the following with suitable examples. i) BFC ii) SXTH iii) UBFX iv) RBIT						8		CO2	2018
4	a	Write the memory map and explain memory access attributes in Cortex M3.						8		CO2	2018
	b	Analyze the following instructions and write the contents of the register the execution of each instruction. Assume R8=0X00000088, R9=0X00000006,R10=0X00001111						8		CO2	2018

		i) RSB.W R8, R9, #0X10 ii) ADD R8, R9,R3 iii) BIC.W R6,R8 #0X06 iv) ORR R8,R9			
5	a	Differentiate the following i) RISC and SISC architecture. ii) Little endian and Big endian architecture.	8	CO3	2018
	b	What are the features of the following I) I²C Bus ii) IrDA iii) Optocoupler iv) 1-wire interface	8	CO3	2018
6	a	What are the different memories types memories used in embedded system design. Explain the role of each.		CO3	2018
	b	Explain the following circuits in an embedded system: I) brown out protection circuits ii) reset circuit		CO3	2018
7	a	Explain the term quality attributes in embedded system development context. What are the different quality attributes to be considered in an embedded system design.	8	CO4	2018
	b	Explain the data flow graph and control flow graph models in the embedded system.	8	CO4	2018
8	a	Explain the different embedded firmware design approach in detail.	8	CO4	2018
	b	Explain the characteristics pf embedded system.	8	CO4	2018
9	a	Explain the concept of deadlock with a block diagram. Mention the different conditions which favours a deadlock condition.	8	CO5	2018
	b	Write a block diagram of IDE environment for an embedded system design explain their function in brief.	8	CO5	2018
10	a	Three processes with process IDs P1,P2,P3 with estimated completion time 10,5,7 ms respectively enters the ready queue together. A new process P4 with completion time 2 ms enters the ready queue after 2ms. Calculate the waiting time for all the processes. Also calculate the average waiting time and average turn around time . The algorithm used is SJF based preemptive scheduling. Assume all the processes contain only CPU operation and no I/O operation involved.	10	CO5	2018
	b	Mention the sequence of operations for embedding the firmware with a programmer and draw the interfacing diagram.	6	CO5	2018

Course Outcome Computation

Academic Year:

Odd / Even semester

INTERNAL TEST					**T1**						**T2**	
Course Outcome	**CO1**		**CO2**		**CO3**		**CO4**		**CO5**		**CO6**	
QUESTION NO	**Q1**	**LV**	**Q2**	**LV**	**Q3**	**LV**	**Q1**	**LV**	**Q2**	**LV**	**Q3**	**LV**
MAX MARKS	10	-	10	-	10	-	10	-	10	-	10	-
USN-1	5	2	10				10	3	9	3	4	1
USN-2	5	2	8	3								
USN-3	7	3	7	3	10	3	8	3	8	3	5	2
USN-4					4	1	10	3	8	3	6	2
USN-5	8	3	6	2	9	3	10	3	8	3		
USN-6							10	3	9	3	4	1
Average CO Attainment		2.5		2.75		2.33		3		3		1.5

LV Threshold : 3:>60%, 2:>=50% and <=60%, 1: <=49%
CO1 Computation :(2+2+2+3)/4 = 10/4=2.5

PO Computation

Program Outcome	PO1		PO3		PO3		PO1		PO12		PO12	
Weight of CO - PO	3		1		3		2		2		3	
Course Outcome	CO1		CO2		CO3		CO4		CO5		CO6	
Test/Quiz/Lab	T1						T2					
QUESTION NO	Q1	LV	Q2	LV	Q3	LV	Q1	LV	Q2	LV	Q3	LV
MAX MARKS	10	-	10	-	10	-	10	-	10	-	10	-
USN-1	5	2	10	3			10	3	9	3	4	1
USN-2	5	2	8	3								
USN-3	7	3	7	3	10	3	8	3	8	3	5	2
USN-4					4	1	10	3	8	3	6	2
USN-5	8	3	6	2	9	3	10	3	8	3		
USN-6							10	3	9	3	4	1
Average CO Attainment		2.5		2.75		2.33		3		3		1.5