Copyright ©2017. cAAS. All rights reserved.

18ECL48: ANALOG CIRCUITS LAB....2

A. LABORATORY INFORMATION....2

1. Lab Overview....2

2. Lab Content....2

3. Lab Material....2

4. Lab Prerequisites:....3

5. General Instructions....3

6. Lab Specific Instructions....4

B. OBE PARAMETERS....4

1. Lab / Course Outcomes....4

2. Lab Applications....5

3. Articulation Matrix....5

4. Curricular Gap and Content....5

C. COURSE ASSESSMENT....6

1. Course Coverage....6

2. Continuous Internal Assessment (CIA)....6

D. EXPERIMENTS....7

Experiment 01 : **COMMON SOURCE JFET/MOSFET AMPLIFIER**....7

Experiment 02 : **BJT COMMON EMITTER AMPLIFIER** 12

Experiment 03 : **COLPITTS OSCILLATOR AND CRYSTAL OSCILLATOR**....16

Experiment 04 :**SECOND ORDER BUTTERWORTH LOW PASS AND HIGH PASS FILTER**....21

Experiment 05 : **ADDER, INTEGRATOR AND DIFFERENTIATOR USING OP-AMP** 27

Experiment 06 :**SCHMITT TRIGGER** 34

Experiment 07 : **R-2R DAC USING OP-AMP37**....37

Experiment 08 : **ASTABLE AND MONOSTABLE MULTIVIBRATOR USING IC 555**....42

Experiment 09 : RC PHASE SHIFT OSCILLATOR AND HARTLEY OSCILLATOR...50

Experiment 10 : **NARROW BAND-PASS FILTER AND NARROW BAND-REJECT FILTER..**
....55

Experiment 11 : **PRECISION HALF AND FULL WAVE RECTIFIER**....59

Experiment 12 :**MONOSTABLE AND ASTABLE MULTIVIBRATOR**....62

Note : Remove “Table of Content” before including in CP Book

Copyright ©2017. cAAS. All rights reserved.

A. LABORATORY INFORMATION

1. Lab Overview

Degree:	B.E	*Program:*	EC
Year / Semester :	2 / 4	*Academic Year:*	2019-20
Course Title:	Analog Circuits Lab	*Course Code:*	18ECL48
Credit / L-T-P:	2/ 2-0-0	*SEE Duration:*	180 Minutes
Total Contact Hours:	36 Hrs	*SEE Marks:*	100 Marks
CIA Marks:	40	*Assignment*	- ------
Course Plan Author:	Arun Kumar R	*Sign*	Dt :
Checked By:		*Sign*	Dt :

2. Lab Content

Unit	Title of the Experiments	Lab Hours	Concept	Blooms Level
1	Design and setup the Common Source JFET/MOSFET amplifier and plot the frequency response	3	Frequency response of JFET/MOSFET	L3
2	Design and set up the BJT common emitter voltage amplifier with and without feedback and determine the gain- bandwidth product, input and output impedances.	3	BJT common emmitter amplification	L3
3	Design and set-up BJT/FET i) Colpitts Oscillator, and ii) Crystal Oscillator	3	Oscillator	L3
4	Design active second order Butterworth low pass and high pass filters.	3	Filters	L3
5	Design Adder, Integrator and Differentiator circuits using Op-Amp	3	Opamp applications	L3
6	Test a comparator circuit and design a Schmitt trigger for the given UTP and LTP values and obtain the hysteresis.	3	comparator	L3
7	Design 4 bit R – 2R Op-Amp Digital to Analog Converter (i) using 4 bit binary input from toggle switches and (ii) by generating digital inputs using mod-16 counter.	3	DAC	L3
8	Design Monostable and a stable Multivibrator using 555 Timer.	3	Multivibrator	L3
9	Simulation using EDA software- RC Phase shift oscillator and Hartley oscillator	3	Oscillator	L3
10	Simulation using EDA software- Narrow Band-pass Filter and Narrow band-reject filter	3	Filter	L3
11	Simulation using EDA software- Precision Half and full wave rectifier	3	Rectifier	L3
12	Simulation using EDA software-Monostable and A stable Multivibrator using 555 Timer.	3	Multivibrator	L3

3. Lab Material

Unit	Details	Available
1	Text books	
	Linear Integrated Circuits‖, D. Roy Choudhury and Shail B. Jain,4thedition, Reprint 2006, New Age International ISBN 978-81-224-3098-1.	
	Operational Amplifiers and Linear IC's‖, David A. Bell, 2nd edition, PHI/Pearson,2004. ISBN 978-81-203-2359-9	
	David A Bell, "Fundamentals of Electronic Devices and Circuits Lab Manual, 5th Edition, 2009, Oxford University Press.	
	Lab Manual	In Lib and dept

Copyright ©2017. cAAS. All rights reserved.

2	Reference books	
i	Ramakant A Gayakwad, –Op-Amps and Linear Integrated Circuits,Pearson, 4th Ed, 2015. ISBN 81-7808-501-1.	In Lib and dept
ii	Robert L. Boylestad and Louis Nashelsky, "Electronics devices and Circuit theory",Pearson, 10th Edition, 2012, ISBN: 978-81-317-6459-6.	In Lib
iii	K. A. Navas, "Electronics Lab Manual", Volume I, PHI, 5th Edition, 2015, ISBN:9788120351424.	In Lib
iv	B Somanathan Nair, –Linear Integrated Circuits: Analysis, Design &Applications, Wiley India, 1st Edition, 2015	In Lib
v	James Cox, –Linear Electronics Circuits and Devices‖, Cengage Learning,Indian Edition, 2008, ISBN-13: 978-07-668-3018-7.	In Lib
3	Others (Web, Video, Simulation, Notes etc.)	In Lib
i	Data Sheet: http://www.ti.com/lit/ds/symlink/tl081.pdf.	
	• https://www.youtube.com/watch?v=CoOOm3NEMfg • https://www.youtube.com/watch?v=6A8otDArahM • https://www.youtube.com/watch?v=1fgw-ONlAcc • https://www.youtube.com/watch?v=YzcKQWwkzWs • https://www.youtube.com/watch?v=lc6QT8VjqVc • https://www.youtube.com/watch?v=sKnLBWA6UdE • https://www.youtube.com/watch?v=BCjnYMNCkGc • https://www.youtube.com/watch?v=5-ohKRWeod4 • https://www.youtube.com/watch?v=Pc1aFloxSMw • https://www.youtube.com/watch?v=XES0QUi8ttY • https://www.youtube.com/watch?v=ypV6gdIJJU4 • https://www.youtube.com/watch?v=iJYm_BGqa1A • https://www.youtube.com/watch?v=k3XgLk2H1w8 • https://www.youtube.com/watch?v=GH-JFXbOcZg • https://www.youtube.com/watch?v=v9sSRF76DDU • https://www.youtube.com/watch?v=ZuFKU9O8FTs • https://www.youtube.com/watch?v=lh768hHRsxg • https://www.youtube.com/watch?v=7jGobEEyD7w	
	Nptel.ac.in for videoes	

4. Lab Prerequisites:

-	-	Base Course:		-	-
SNo	Course Code	Course Name	Topic / Description	Sem	Remarks
1	18ELN14/24	Basic Electronics	OPAMP / Rectifiers / BJT & FET working operation	1/2	

Note: If prerequisites are not taught earlier, GAP in curriculum needs to be addressed. Include in Remarks and implement in B.5.

5. General Instructions

SNo	Instructions	Remarks
1	Observation book and Lab record are compulsory.	
2	Students should report to the concerned lab as per the time table.	
3	After completion of the program, certification of the concerned staff in-charge in	

Copyright ©2017. cAAS. All rights reserved.

	the observation book is necessary.	
4	Student should bring a notebook of 100 pages and should enter the readings /observations into the notebook while performing the experiment.	
5	The record of observations along with the detailed experimental procedure of the experiment in the Immediate last session should be submitted and certified staff member in-charge.	
6	Should attempt all problems / assignments given in the list session wise.	
7	When the experiment is completed, should disconnect the setup made by them, and should return all the components/instruments taken for the purpose.	
8	Any damage of the equipment or burn-out components will be viewed seriously either by putting penalty or by dismissing the total group of students from the lab for the semester/year	
9	Completed lab assignments should be submitted in the form of a Lab Record in which you have to write the Components required, Theory, Procedure, tabular column and output for various inputs given	

6. Lab Specific Instructions

SNo	Specific Instructions	Remarks
1	Rigup the circuits as shown in the lab manual for each experiment	
2	Turn on the supply and Apply the proper input when it is required	
3	Observe the output , note down the readings and compare it with theoretical value	
4	Plot the graph using graph/ semilog sheets	
5	Turn off the supply & Disconnect the ciruit	

B. OBE PARAMETERS

1. Lab / Course Outcomes

#	COs	Teach. Hours	Concept	Instr Method	Assessment Method	Blooms ' Level
1	Design the circuits using BJT and FET	12	BJT / FET performance characteristics	Lecture and Demonstrate	Test and Viva	L3
2	Design the circuits using Op-Amp	12	OPAMPs for different applications	Lecture and Demonstrate	Test and Viva	L3
3	Simulate and analyze analog circuits that uses transistor and ICs for different electronic applications.	12	555 timer and Simulation	Lecture and Demonstrate	Test and Viva	L3

Note: Identify a max of 2 Concepts per unit. Write 1 CO per concept.

2. Lab Applications

SNo	Application Area	CO	Level

Dept EC
Prepared by Checked by Approved

Copyright ©2017. cAAS. All rights reserved.

1	frequency-determining component, a wafer of quartz crystal or ceramic with electrodes connected to it.	CO1	L3
2	Used in speech processing for communications (radio) applications & audio compression.	CO1	L3
3	Used in RF,radio, small power supply units, medical field etc	CO1	L3
4	In some Capacitor to power the high-side NMOS driver.	CO1	L3
5	Apply voltage divider bias to find gain bandwidth & frequency response	CO1	L3
6	Used in buffer amplifier,electronic switch, phase shift oscillator etc	CO1	L3
7	widely used for switching and amplifying electronic signals in the electronic devices.	CO1	L3
8	Oscillators is used in microprocessor for clock circuits	CO1	L3
9	used in low-cost design devices and mobile devices	CO2	L3
10	Differentiator is used in signal amplifier	CO2	L3
11	Integrator used in wave shaping circuit	CO2	L3
12	Active filters used in demodulator circuit	CO2	L3
13	R-2R ladder network used in DAC	CO2	L3
14	Multivibrators are used for time delay calculation	CO3	L3
15	Used as external triggers	CO3	L3

Note: Write 1 or 2 applications per CO.

3. Articulation Matrix

(CO – PO MAPPING)

-	Course Outcomes	Program Outcomes												
#	COs	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	Level
18EC48.1	Design the circuits using BJT and FET	3	3	2						2	2			L3
18EC48.2	Design the circuits using Op-Amp and 555 timer for different applications	3	3	2						2	2			L3
18EC48 .3	Simulate and analyze analog circuits that uses transistor and ICs for different electronic applications.	3	3	2		2				2	2			L3

Note: Mention the mapping strength as 1, 2, or 3

4. Curricular Gap and Content

SNo	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1					
2					
3					
4					
5					

Copyright ©2017. cAAS. All rights reserved.

Note: Write Gap topics from A.4 and add others also.

Note: Anything not covered above is included here.

C. COURSE ASSESSMENT

1. Course Coverage

Unit	Title	Teaching Hours	No. of question in Exam							CO	Levels
			CIA-1	CIA-2	CIA-3	Asg-1	Asg-2	Asg-3	SEE		
1	Design and setup the Common Source JFET/MOSFET amplifier and plot the frequency response	03	1	-	-	-	-	-	1	CO1	L4
2	Design and set up the BJT common emitter voltage amplifier with and without feedback and determine the gain- bandwidth product, input and output impedances.	03	1	-	-	-	-	-	1	CO1	L4
3	Design and set-up BJT/FET i) Colpitts Oscillator, and ii) Crystal Oscillator	03	2	-	-	-	-	-	2	CO1	L4
4	Design active second order Butterworth low pass and high pass filters.	03	2	-	-	-	-	-	2	CO2	L4
5	Design Adder, Integrator and Differentiator circuits using Op-Amp	03	2	-	-	-	-	-	2	CO2	L4
6	Test a comparator circuit and design a Schmitt trigger for the given UTP and LTP values and obtain the hysteresis.	03	2	-	-	-	-	-	2	CO2	L4
8	Design Monostable and a stable Multivibrator using 555 Timer.	03	-	2	-	-	-	-	2	CO2	L4
9	Simulation using EDA software- RC Phase shift oscillator and Hartley oscillator	03	-	2	-	-	-	-	2	CO2	L4
10	Simulation using EDA software- Narrow Band-pass Filter and Narrow band-reject filter	03	-	2	-	-	-	-	2	CO3	L4
11	Simulation using EDA software- Precision Half and full wave rectifier	03	-	2	-	-	-	-	2	CO3	L4
12	Simulation using EDA software- Monostable and A stable Multivibrator using 555 Timer.	03	-	2	-	-	-	-	2	CO3	L4
-	**Total**	**36**	**10**	**11**	-	-	-	-	**21**	-	-

Note: Write CO based on the theory course.

2. Continuous Internal Assessment (CIA)

Evaluation	Weightage in Marks	CO	Levels
CIA Exam – 1	30	CO1, CO2	L2
CIA Exam – 2	30	CO3,C04	L4
CIA Exam – 3	30	CO4	L4

Copyright ©2017. cAAS. All rights reserved.

Assignment - 1	05	CO1, CO2	L2
Assignment - 2	05	CO3,C04	L4
Assignment - 3	05	CO4	L4
Other Activities – define – Slip test		CO1 to CO4	L2, L3, L4 . ..
Final CIA Marks	**40**	-	-

-

SNo	Description	Marks
1	Observation and Weekly Laboratory Activities	05 Marks
2	Record Writing	10 Marks for each Expt
3	Internal Exam Assessment	20 Marks
4	Internal Assessment	40 Marks
5	SEE	60Marks
-	**Total**	**100 Marks**

D. EXPERIMENTS

Experiment 01 : COMMON SOURCE JFET/MOSFET AMPLIFIER

-	Experiment No.:	1	Marks	10	Date Planned		Date Conducted	
1	Title	**COMMON SOURCE JFET/MOSFET AMPLIFIER**						
2	Course Outcomes	Design analog circuits using BJT/FETs and evaluate their performance characteristics.						
3	Aim	To design, setup and plot the frequency response of Common Source JFET amplifier and obtain the bandwidth.						
4	Material / Equipment Required							

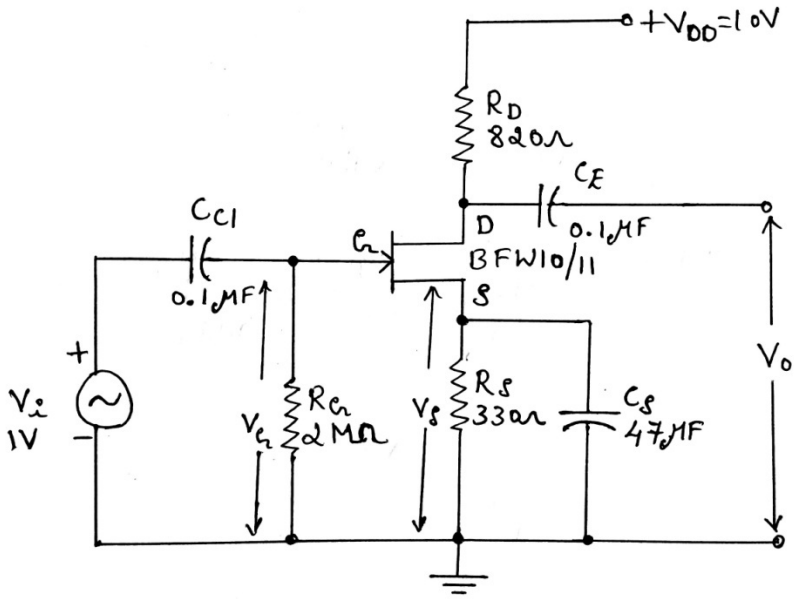
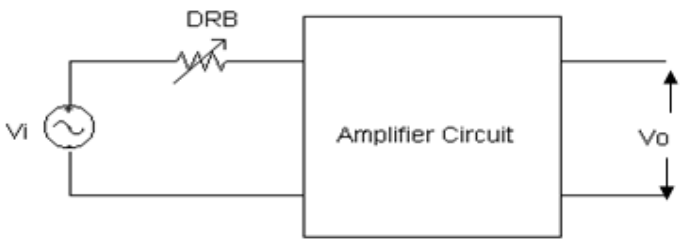
Sl. No.	Particulars	Range	Quantity
1.	JFET (BFW10)	-	1
2.	Capacitor	47μF,0.1μF	1,2
3.	Resistor	2MΩ, 820Ω,330Ω	1,1
4.	Power Supply	0-30V	1
5.	Signal Generator	2MHz	1
6.	CRO	-	1
7.	Multimeter	-	1
8.	Spring Board	-	1
9.	Connecting Wires	-	-

5	Theory, Formula, Principle, Concept	The JFET gate voltage V_g is biased through the potential divider network set up by the resistors R_1 and R_2 and is biased to operate within its saturation region which is equivalent to the active region of the BJT.

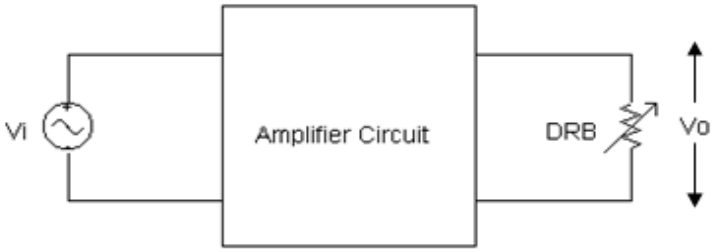
Copyright ©2017. cAAS. All rights reserved.

		Unlike the BJT, the junction FET takes virtually no input gate current allowing the gate to be treated as an open circuit. Then no input characteristics curves are required. Since the n-channel JFET is a depletion mode device, a negative gate voltage with respect to the source is required to modulate or control the drain current. This negative voltage can be provided by biasing from a separate power supply voltage or by self biasing arrangements as long as steady current flows through the JFET even when there is no input signal present and V_g maintains a reverse bias of the gate source p-n junction. The input signal of the common source JFET amplifier is applied between the gate terminals with a constant value of gate voltage applied. The JFET operates within its ohmic region acting like a linear resistive device. The drain circuit contains the load resistor R_D. The output voltage is developed across this load resistance.
6	Procedure, Program, Activity, Algorithm, Pseudo Code	•Check all the components and equipments for their good working condition. •Connections are made as shown in the circuit diagram. •By keeping the voltage knobs in minimum position and current knob in maximum position switch on the power supply. •By disconnecting the AC source measure the quiescent point. •**To find frequency response:** •Connect the AC source. Keeping the frequency of the Ac source in mid band region (say 10 kHz) adjust the amplitude to get the distortion less output. Note down the amplitude of the input signal. •Keeping the input amplitude constant, Vary the frequency in suitable steps and note down the corresponding output amplitude. •Calculate A_V and gain in decibels. Plot a graph of frequency V_S gain in dB. From the graph calculate f_L, f_H and band width. •Calculate figure of merit. •**To find the input impedance (Z_i):**

Copyright ©2017. cAAS. All rights reserved.

		•Connections are made as shown in the diagram. •Keeping the DRB in its minimum position, apply input signal at mid band frequency (say 10kHz) and adjust the amplitude of the input signal to get distortion less output. Note down the output amplitude. •Vary the DRB until the output amplitude becomes half of its previous value. The corresponding DRB value gives the input impedance. **•To find the output impedance (Z_o):** •Connections are made as shown in the diagram. •Keeping the DRB in its maximum position, apply input signal at mid band frequency (say 10k Hz) and adjust the amplitude of the input signal to get distortion less output. Note down the output amplitude. Vary the DRB until the output amplitude becomes half of its previous value. The corresponding DRB value gives the output impedance.
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	 **Circuit to find input impedance (Z_i):**  **Circuit to find output impedance (Z_o):**

Copyright ©2017. cAAS. All rights reserved.



8 Observation Table, Look-up Table, Output

Frequency in Hz	V_o in Volt	$A_V = \frac{V_O}{V_I}$	**Gain in dB=20 log** A_V

9 Sample Calculations

Given $V_{DD}=10\,V$, $V_{GS(off)}=-4\,V$, $I_{DSS(max)}=12\,\text{mA}$, $R_G=2\,M\Omega$

Formulae, $$I_D=I_{DSS}\left(\frac{1-V_{GS}}{V_{GS(off)}}\right)^2 \quad \text{-----(1)}$$

When $V_G=0$, Then $V_S=-V_{GS}$

But $V_S=I_D\times R_S$

When $V_G=0$, $I_D=I_{DSS}$

$V_S=I_{DSS}\times R_S$

$I_{DSS}\times R_S=-V_{GS(off)}$

$$R_S=\frac{-(-4)}{12\,\text{mA}}=333\,\Omega$$

Choose $R_S=330\,\Omega$

From Eq. (1)

$$I_D=I_{DSS}\left(\frac{1-I_D R_S}{V_{GS(off)}}\right)^2$$

$$I_D=I_{DSS}\left(\frac{1+I_D^2\times R_S^2}{16}-\frac{I_D R_S}{2}\right)$$

Copyright ©2017. cAAS. All rights reserved.

$$I_D = 12\times10^{-3}\left(\frac{1+I_D^2\times330^2}{16}-\frac{I_D\times330}{2}\right)$$

$$81.675\,I_D^2-2.98\,I_D+12\times10^{-3}=0$$

$I_D = 4.6\,\text{mA}$ or $I_D = 31.9\,\text{mA}$

Since I_D cannot be greater than I_{DSS}, Choose $I_D = 4.6\,\text{mA}$

Assume $V_{DS} = 50\%V_{DD}$, $V_{DS} = 5\,V$

Applying KVL to output circuit

$$V_{DD} = I_D R_D + V_{DS} + I_D R_S$$

$$V_{DD} - V_{DS} = I_D(R_D + R_S)$$

$$\frac{10\,V-5\,V}{I_D} = (R_D+R_S)$$

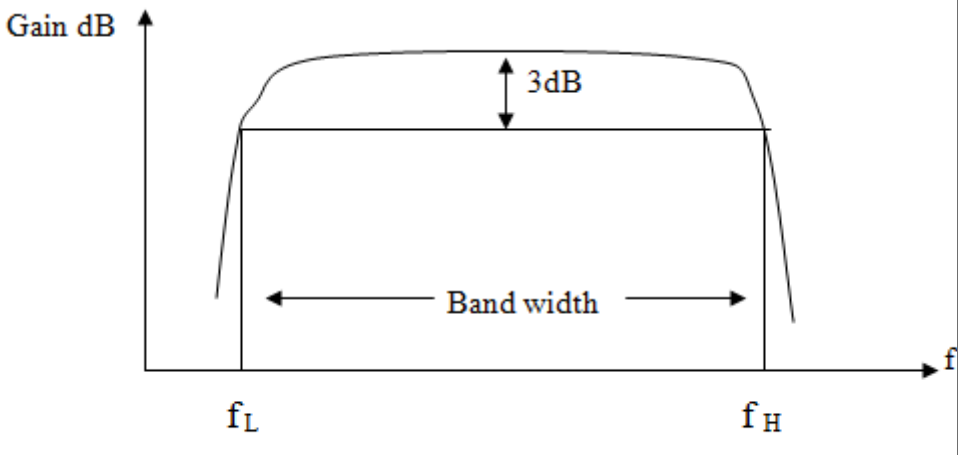
$$\frac{5\,V}{4.6\,\text{mA}} = (R_D+R_S)$$

$$R_D = \frac{5\,V}{4.6\,\text{mA}} - 330\,\Omega$$

$$R_D = 756\,\Omega$$

Choose $R_D = 820\,\Omega$

10 Graphs, Outputs



f_L = Lower cutoff frequency f_H = Higher cutoff frequenc

11 Results & Analysis

1. Quiescent point: V_{DS} = _____V and I_D = _____mA.
2. Voltage Gain (A_V) = _____ (in mid band region).
3. Bandwidth (BW) = _____ Hz.
4. figure of merit (FM) = _____ Hz.
5. Input impedance (Z_i) = _____Ω, Output Impedance (Z_o)

Copyright ©2017. cAAS. All rights reserved.

		= _____
12	Application Areas	Used in CRO used in electronic voltmeter
13	Remarks	
14	Faculty Signature with Date	

Experiment 02 : BJT COMMON EMITTER AMPLIFIER

-	**Experiment No.:**	2	**Marks**	10	**Date Planned**		**Date Conducted**	
1	Title	**BJT COMMON EMITTER AMPLIFIER**						
2	Course Outcomes	Design analog circuits using BJT/FETs and evaluate their performance characteristics.						
3	Aim	To design and set up the BJT common emitter amplifier using voltage divider bias with and without feedback and determine the gain- bandwidth product from its frequency response.						
4	Material Equipment Required	/						

Sl. No.	**Particulars**	**Range**	**Quantity**
1.	Transistor (SL100/CL100)	-	1
2.	Resistor	47KΩ, 1.8KΩ,8.2KΩ,470Ω	1,1,1,1
3.	Capacitor	0.47μF, 47μF	2,1
4.	Signal Generator	20MHz	1
5.	CRO	-	1
6.	Power Supply	0-30V	1
7.	Multimeter	-	1
8.	Spring Board	-	1
9.	Connecting Wires	-	-

5	Theory, Formula, Principle, Concept	The single staged common emitter amplifier circuit uses voltage divider biasing. This type of biasing arrangement uses two resistors as a potential divider network across the supply with their centre point supplying the required base bias voltage to the transistor. Voltage divider biasing is commonly used in the design of bipolar transistor amplifier circuits. In common emitter amplifier circuits, capacitors C_1 and C_2 are used as coupling capacitors to separate the AC signals from the DC biasing voltage. This ensures that the biasing condition set up for the circuit to operate correctly is not affected by any additional amplifier stages as the capacitors will only pass AC signals and block any DC component. The output AC signal is then superimposed on the biasing of the following stages. Also a bypass capacitor C_E is included in the emitter leg circuit.

Copyright ©2017. cAAS. All rights reserved.

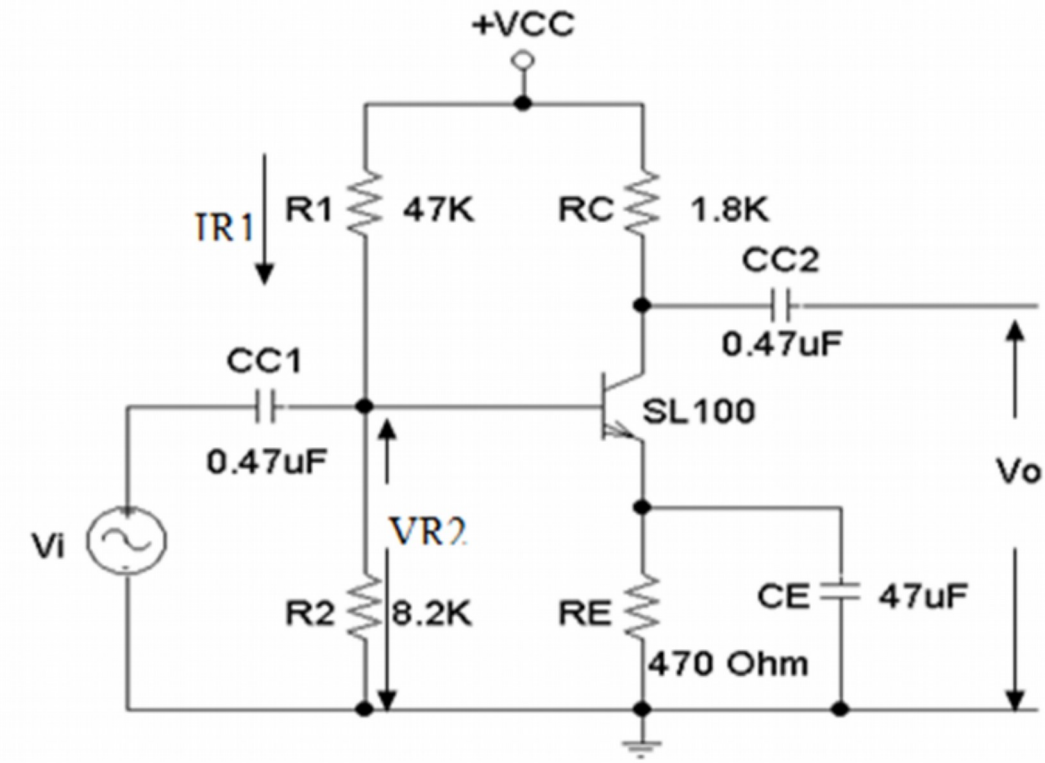
6	Procedure, Program, Activity, Algorithm, Pseudo Code	Check all the components and equipments for their good working condition. Connections are made as shown in the circuit diagram. By keeping the voltage knobs in minimum position and current knob in maximum position switch on the power supply. By disconnecting the AC source measure the quiescent point. **To find frequency response:** 1. Connect the AC source. Keeping the frequency of the Ac source in mid band region (say 10 kHz) adjust the amplitude to get the distortion less output. Note down the amplitude of the input signal. 2. Keeping the input amplitude constant, Vary the frequency in suitable steps and note down the corresponding output amplitude. 3. Calculate $A_V$and gain in decibels. Plot a graph of frequency Vs gain in dB. From the graph calculate f_L, f_H and band width. 4. Calculate figure of merit. **To find the input impedance (Z_i):** 1. Connections are made as shown in the diagram. 2. Keeping the DRB in its minimum position, apply input signal at mid band frequency (say 10kHz) and adjust the amplitude of the input signal to get distortion less output. Note down the output amplitude. 3. Vary the DRB until the output amplitude becomes half of its previous value. The corresponding DRB value gives the input impedance. **To find the output impedance (Z_O):** 1. Connections are made as shown in the diagram. 2. Keeping the DRB in its maximum position, apply input signal at mid band frequency (say 10k Hz) and adjust the amplitude of the input signal to get distortion less output. Note down the output amplitude. 3. Vary the DRB until the output amplitude becomes half of its previous value. The corresponding DRB value gives the output impedance. **Result:**

Copyright ©2017. cAAS. All rights reserved.

1. Quiescent point: V_{CE}= V, I_C= mA.
2. Voltage Gain (A_V) = _____ (in mid band region).
3. Bandwidth (BW) = _____ Hz.
4. Figure of merit (FM) = _____ Hz.
5. Input impedance (Z_i) = _____, Output Impedance (Z_O) = _____.

ΩΩ

7 Block, Circuit, Model Diagram, Reaction Equation, Expected Graph



8 Observation Table, Look-up Table, Output

Frequency in Hz	V_o in Volt	$A_V = \frac{V_O}{V_I}$	**Gain in dB=20 log** A_V

9 Sample Calculations

Design:

Given $V_{CE}=5V$ and $I_{C2}=2\text{mA}$ Assume β=100

$V_{CC}=2V_{CE}=10V$,

Copyright ©2017. cAAS. All rights reserved.

Let $V_{RE}=10\%V_{CC}=1\,V$

$$R_E=\frac{V_{RE}}{I_C+I_B}$$

$$I_B=\frac{I_C}{\beta}=\frac{2\,\text{mA}}{100}=20\,\mu A$$

$$R_E=\frac{1}{2\,\text{mA}+20\,\mu A}=495\,\Omega$$

Choose $R_E=470\,\Omega$

Apply KVL to Collector Loop

$$V_{CC}-I_C R_C-V_{CE-¿V_E=0}¿$$

$$R_C=V_{CC}-\frac{V_{CE-¿V_E}}{I_C}=\frac{10-5-1}{2m}¿$$

$R_C=2\,K\,\Omega$ Choose $R_C=1.8\,\text{K}\Omega$

Let $\text{IR}_1=10\,\text{IB}=10\times 20\,\mu A=200\,\mu A$

$V_{R2}=V_{BE}+V_E=0.6+1=1.6\,V$ (Since transistor is silicon make V_{BE} = 0.6 V)

$$R_2=\frac{V_{R2}}{\text{IR}_1-\text{IB}}=\frac{1.6\,V}{200\,\mu+20\,\mu}=7.2\,K\,\Omega$$

Choose $R_2=8.2\,\text{K}\Omega$

$$R_1=\frac{V_{CC}-V_{R2}}{\text{IR}_1}=\frac{10-1.6}{200\,\mu A}=42\,K\,\Omega$$

Choose $R_1=47\,\text{K}\Omega$

The condition is that X_{CE} << R_E

Let $X_{CE}=\frac{R_E}{10}$

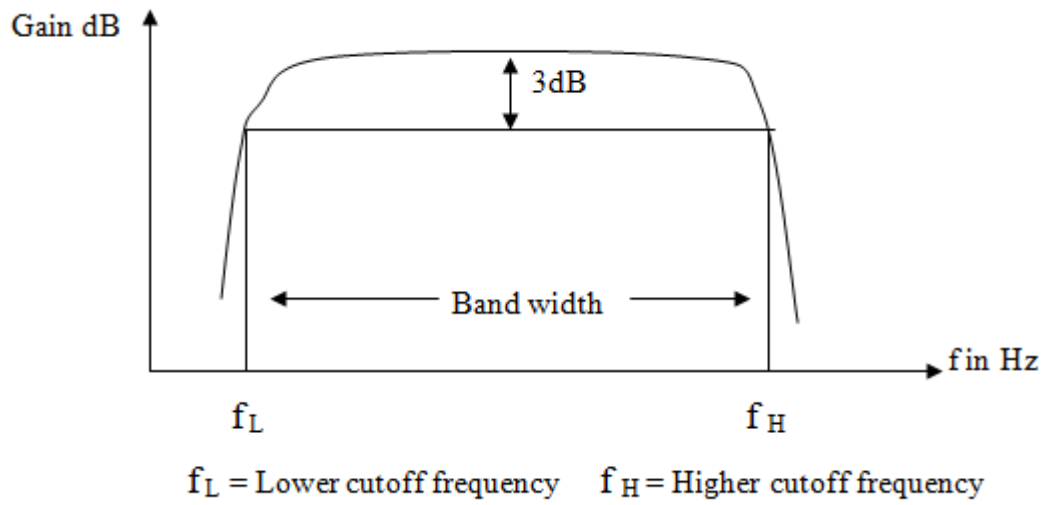
$$\frac{1}{2\pi f C_E}=\frac{470}{10}$$ Let f=100Hz

$$C_E=33\,\mu F$$

Choose $C_E=47\,\mu F$

Also $C_{C1}=C_{C2}=0.47\,\mu\text{F}$

Copyright ©2017. cAAS. All rights reserved.

10	Graphs, Outputs	
11	Results & Analysis	Quiescent point: V_{CE}=¿¿¿, I_C=¿¿¿. 1. Voltage Gain (A_V) = _____ (in mid band region). 2. Bandwidth (BW) = _____ Hz. 3. Figure of merit (FM) = _____ Hz. 4. Input impedance (Z_i) = _____, Output Impedance (Z_O) = _____.
12	Application Areas	Used in low noise amplifiers used in radio frequencies transceiver circuits
13	Remarks	
14	Faculty Signature with Date	

Experiment 03 : COLPITTS OSCILLATOR AND CRYSTAL OSCILLATOR

-	**Experiment No.:**	3	**Marks**	10	**Date Planned**		**Date Conducted**	
1	Title	**COLPITTS OSCILLATOR AND CRYSTAL OSCILLATOR**						
2	Course Outcomes	Design analog circuits using BJT/FETs and evaluate their performance characteristics.						
3	Aim	To Design and set-up the following tuned oscillator circuits using BJT, and determine the frequency of oscillation. (a) Colpitts Oscillator (b) Crystal Oscillator						
4	Material / Equipment Required							

Sl. No.	Particulars	Range	Quantity
1.	Transistor (SL100/CL100)	-	1
2.	Crystal	2MHz	1
3.	Resistor	47KΩ, 1.8KΩ,8.2KΩ,470Ω	1,1,1,1
4.	Capacitor	0.47μF,47 μF	2,1
5.	Decade Capacitance Box	-	2

Copyright ©2017. cAAS. All rights reserved.

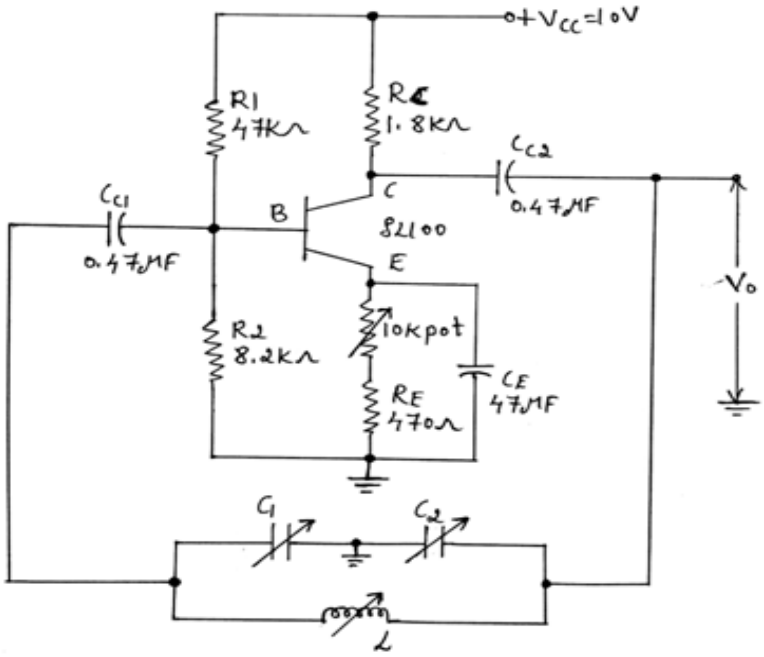
		6.	CRO	-	1
		7.	Power Supply	0-30V	1
		8.	Multimeter	-	1
		9.	Spring Board	-	1
		10.	Connecting Wires	-	-

CRYSTAL OSCILLATOR

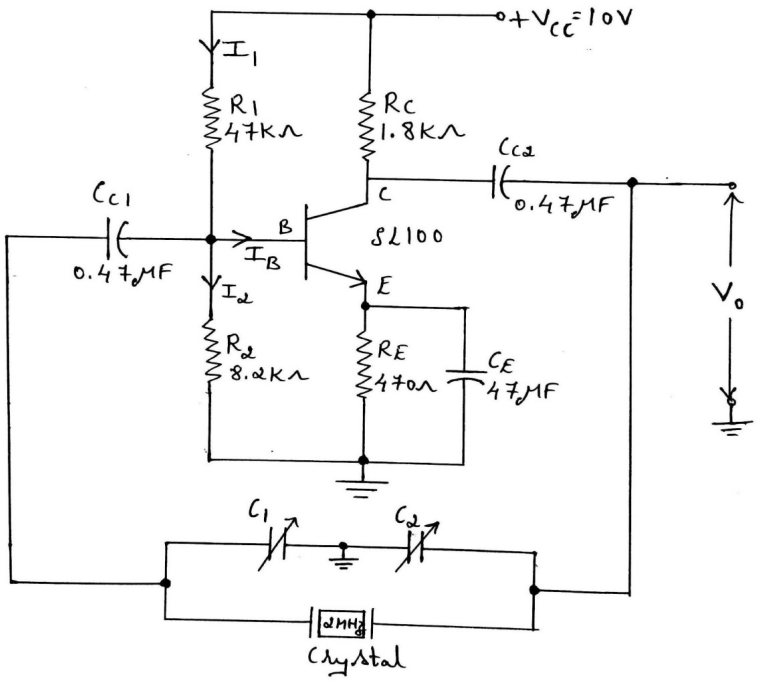
		Sl. No.	**Particulars**	**Range**	**Quantity**
		1.	Transistor (SL100/CL100)	-	1
		2.	Crystal	2MHz	1
		3.	Resistor	47KΩ, 1.8KΩ,8.2KΩ,470Ω	1,1,1,1
		4.	Capacitor	0.47μF,47 μF	2,1
		5.	Decade Capacitance Box	-	2
		6.	CRO	-	1
		7.	Power Supply	0-30V	1
		8.	Multimeter	-	1
		9.	Spring Board	-	1
		10.	Connecting Wires	-	-

5	Theory, Formula, Principle, Concept	**Colpitts Oscillator:** A Colpitts oscillator is an electronic oscillator that uses a combination of inductor and capacitor to produce an output of certain frequency. It consists of a gain device with its output connected to the input in a feedback loop consisting of a parallel LC circuit. The Colpitts oscillator uses a capacitance voltage divider network as its feedback source. The two capacitors are connected across a single common inductor. The advantage of this type of capacitance circuit configuration is that with less and mutual inductance within the tank circuit, frequency stability of the oscillator is improved along with more simple design. **CRYSTAL OSCILLATOR:** Crystal oscillators are used in order to get stable sinusoidal signals despite of variations in temperature, humidity, transistor and circuit parameters. A piezo electric crystal is used in this oscillator as resonant tank circuit. Crystal works under the principal of piezo-electric effect. i.e., when an AC signal applied across the crystal, it vibrates at the frequency of the applied voltage. Conversely if the crystal is forced to vibrate it will generate an AC signal. Commonly used crystals are Quartz, Rochelle salt etc.
6	Procedure, Program, Activity,	1. Connections are made as shown in the diagram.

Copyright ©2017. cAAS. All rights reserved.

	Algorithm, Pseudo Code	2. The quiescent point of the amplifier is verified for the designed value. 3. Observe the output waveform on CRO and measure the frequency. 4. Verify the output frequency with the theoretical frequency. **Crystal oscillator** 5. Connections are made as shown in the diagram. 6. The quiescent point of the amplifier is verified for the designed value. 7. Observe the output wave form on CRO and measure the frequency. 8. Verify the frequency with the crystal frequency.
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	 Crystal oscillator:

Copyright ©2017. cAAS. All rights reserved.

		
8	Observation Table, Look-up Table, Output	
9	Sample Calculations	**Colpitts Oscillator tank circuit design:** Choose A=2, $f_o = 100\,\text{KHz}$ $f_o = \frac{1}{2\pi\sqrt{L C_{eq}}}$ ------(c) $C_{eq} = L_1 + L_2$ --------(d) Condition for oscillation $A\beta \geq 1$ $A = \frac{C_1}{C_2}$ => $C_1 = 2C_2$ Find C_{eq} from (d) and L from (c) crystal oscillator: **Design:** Given, $V_{CE} = 5V$ and $I_C = 2\,\text{mA}$, Assume ✔ = 100 $V_{CC} = 2V_{CE} = 2\times 5 = 10V$ Let $V_{RE} = 10\%V_{CC} = 1V$

Copyright ©2017. cAAS. All rights reserved.

$$R_E = \frac{V_{RE}}{I_C + I_B}$$

$$I_B = \frac{I_C}{\beta} = \frac{2\,\text{mA}}{100} = 20\,\mu A$$

$$R_E = \frac{1}{2\,\text{mA} + 20\,\mu} = 495\,\Omega$$

Choose $R_E = 470\,\Omega$

Apply KVL to collector loop

$$V_{CC} - I_C R_C - V_{CE} - V_E = 0$$

$$R_C = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{10 - 5 - 1}{2m}$$

$R_C = 2\,\text{K}\Omega$ Choose $R_C = 1.8\,\text{K}\Omega$

Let $\text{IR}_1 = 10\,I_B = 10 \times 20\,\mu\text{A} = 200\,\mu\text{A}$

$\text{VR}_2 = V_{BE} + V_E = 0.6 + 1 = 1.6\,V$ (Since transistor is silicon make $V_{BE} = 0.6\,V$)

$$R_2 = \frac{\text{VR}_1}{\text{IR}\,1 - I_B} = \frac{1.6}{200\,\mu\text{A} + 20\,\mu\text{A}}$$

R_2 = 7.2 K Choose R_2 = **8.2 K**

$$R_1 = \frac{(V_{CC} - \text{VR}_2)}{\text{IR}_1} = \frac{(10 - 1.6)}{200\,\mu\text{A}} \quad R_1 = 42\,\text{K}\Omega$$ Choose $R_1 = 47\,\text{K}\Omega$

$X_{CE} \ll R_E$

$$X_{CE} = \frac{R_E}{10}$$

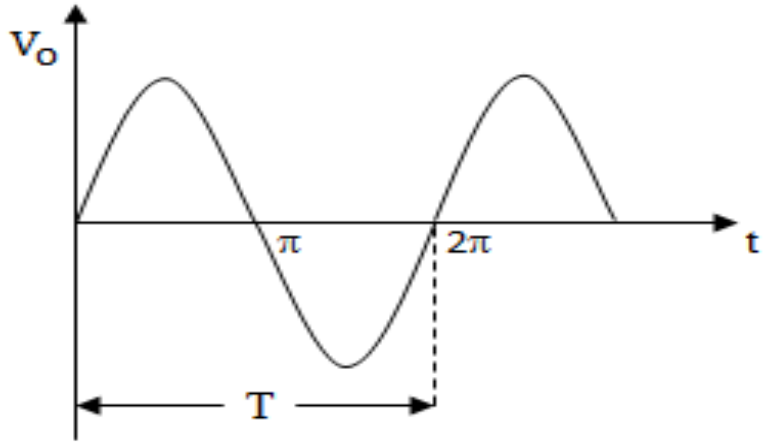
$$\frac{1}{2\pi f C_E} = \frac{470}{10}$$

Let f = 100 Hz

C_E = 33 ↄF Choose R_1 = **47** ↄ**F**

Choose CC_1 = CC_2 = **0.47** ↄ**F**

Copyright ©2017. cAAS. All rights reserved.

10	Graphs, Outputs	
11	Results & Analysis	Colpitts Oscillator: Theoretical frequency (f) = _____ Hz Practical frequency (f) = _____Hz. For Crystal = _____ Hz. For Practical = _____ Hz.
12	Application Areas	
13	Remarks	
14	Faculty Signature with Date	

.....

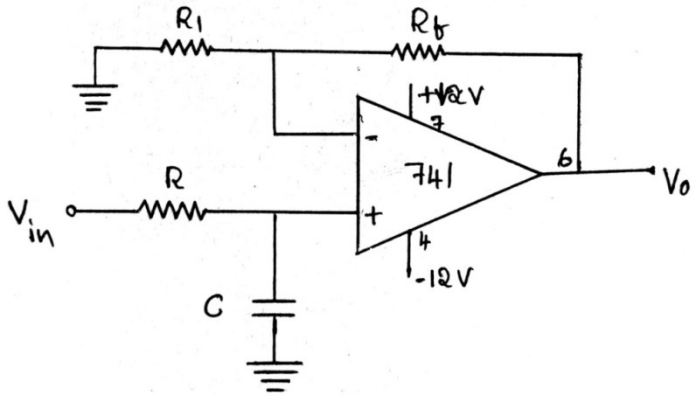
Experiment 04 :SECOND ORDER BUTTERWORTH LOW PASS AND HIGH PASS FILTER

-	**Experiment No.:**	4	**Marks**	10	**Date Planned**		**Date Conducted**	
1	Title	**SECOND ORDER BUTTERWORTH LOW PASS AND HIGH PASS FILTER**						
2	Course Outcomes	Design analog circuits using OPAMPs and 555 timerfor different applications						
3	Aim	To design a second order butter worth second order low pass and high pass filter for a given cut off frequency and draw the frequency response.						
4	Material / Equipment Required	**Components Required:** 1. IC 741 Op-Amp 2. Resistors – As per the design 3. Capacitor – As per the design 4. Power supply 5. Signal generator 6. CRO						
5	Theory, Formula, Principle, Concept	**Low pass filter:**						

Copyright ©2017. cAAS. All rights reserved.

Low pass filter allows only low frequency signal to pass through them. A low pass filter can be a combination of capacitance, inductance or resistance to produce high attenuation above a specified frequency & little or no attenuation below that frequency .The frequency at which the transition occurs is called cut-off frequency.

- A first order low pass Butterworth filter uses RC network for filtering. The op-Amp is used in non-inverting configuration.



- The first order filter can be connected to second order LPF by using additional RC network as shown in fig1.

2nd order:

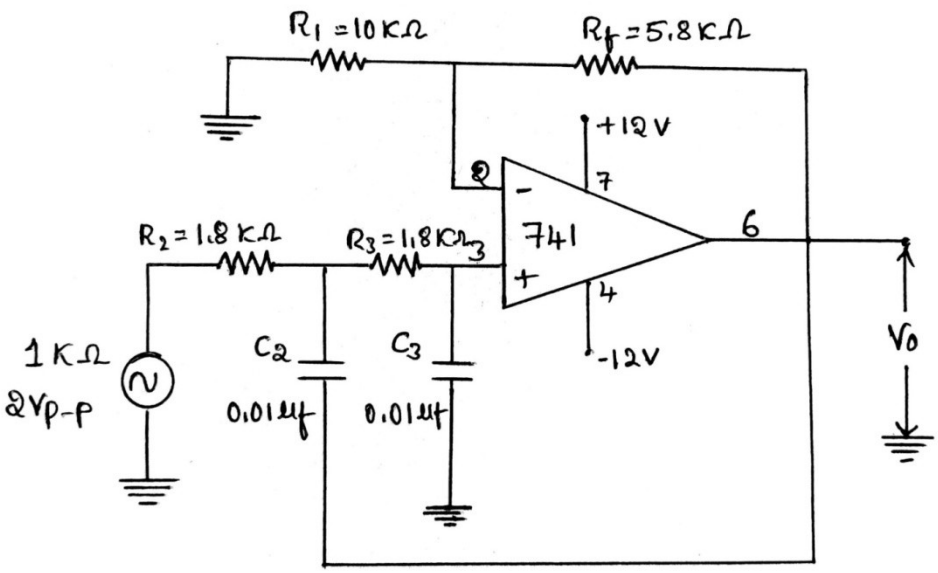
- The stop-band response in 2nd order LPF is 40dB/decade. At low frequency, both capacitors appear open and the circuit becomes a non-inverting amplifier $\left(\because X_C = \frac{1}{2\pi FC}\right)$
- As frequency increase, the gain eventually starts to decrease until-it is down 3dB at the cutoff frequency. As frequency increase the cut off frequency, the o/p is attenuated.

b) High pass filter:

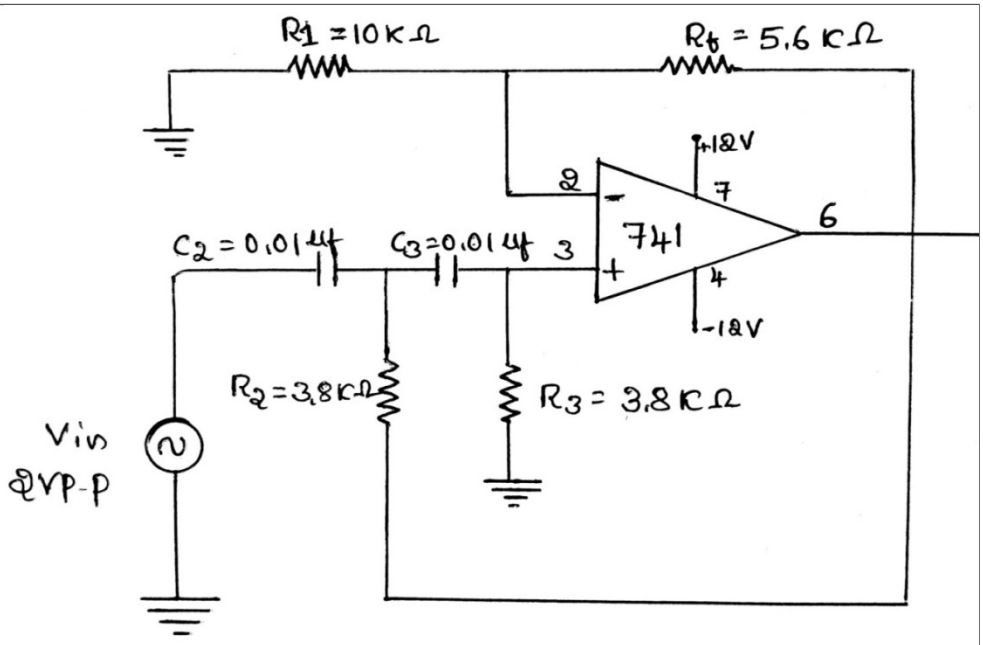
High pass filter passes high frequency signals to pass through it. Again frequency sensitive components such as capacitors & inductors are used in conjunction with the resistors.

The first order high pass filter is formed from first order low pass filter by interchanging the R&C components &second order HPF filter can be obtained from 2nd order LPF by interchanging R&C as shown in Fig3.

Copyright ©2017. cAAS. All rights reserved.

		Here as frequency increase, the capacitors act as short & the circuit behaves as amplifier with gain A_f but when the frequency is low, the capacitor act as open circuit & hence very little signal passes through the circuit.
6	Procedure, Program, Activity, Algorithm, Pseudo Code	1. Rig up the circuits as show in the diagrams 2. apply the input as specified 3. vary the input signal frequency and note down the output voltages and calculate the gain convert the gain in db 4. plot the graph frequency/ gain in db and observe the cut-off points and calculate the roll off
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	 **a) High pass filter** **Circuit Diagram:**

Copyright ©2017. cAAS. All rights reserved.



8 Observation Table, Look-up Table, Output

$$V_i = 2V_{p-p}$$

	Frequency (H_Z)	V_O **(V)**	$A_V = \frac{V_O}{V_I}$	**20 LOG** A_V	

9 Sample Calculations

LPF:

The higher cutoff frequency that is the frequency at which signal falls (3dB) below is given by

for LPH: $f_H = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$

HPF:

The lower cutoff frequency that is the frequency at which signal strength falls 3dB below this is given by

Copyright ©2017. cAAS. All rights reserved.

$$f_L = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$$

b) Low pass filter

Design 2nd order LPF to obtain f_H = 9KHz

Solution:

$$f_H = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$$

Let $R_2 = R_3$ = R & C_2 = C3= C

$$\therefore f_H = \frac{1}{2\pi RC}$$

Choose C = 0.01μf

$$\therefore R = \frac{1}{2\pi f_H C} = \frac{1}{2\pi * 9K * 0.01\,\mu f} = 1.768k\Omega$$

$\therefore$ Choose R = 1.8KΩ

The pass band gain of 2^{nd} order filter = 1.586

$$A_f = 1 + \frac{R_f}{R_1} = 1.586$$

$$\therefore \frac{R_f}{R_1} = 0.586$$

Let R_1 = 10KΩ & hence R_f = 0.586

R_1 ==> R_f =5.86KΩ

Design:

Design HPF to obtain f_H = 4 KHz

Solution:

$$f_H = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$$

Let $R_2 = R_3$ = R & C_2 = C3= C & hence

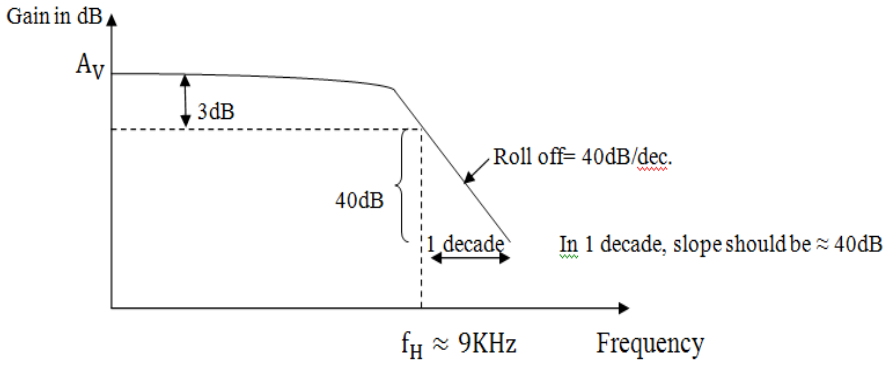
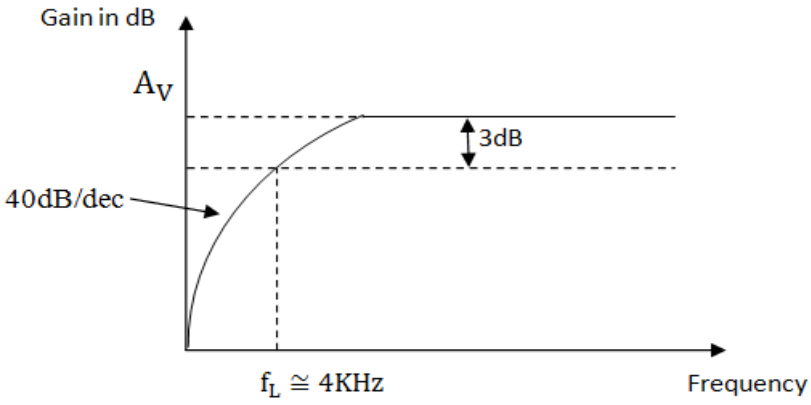
$$f_H = \frac{1}{2\pi RC}$$

Let C =0.01μf

$$\therefore R = \frac{1}{2\pi f_H c} = \frac{1}{2\pi * 4K * 0.01\,\mu f} = 3.9K\Omega$$

Hence choose R =3.8KΩ

Copyright ©2017. cAAS. All rights reserved.

		The pass band gain of 2nd order filter is 1.586 $\therefore \quad A_f = 1 + \frac{R_f}{R_1} = 1.586$ $\frac{R_f}{R_1} = 0.586$ Let R_1 =10KΩ & hence R_f =0.586 R_1 ==> R_f = 5.8KΩ
10	Graphs, Outputs	 
11	Results & Analysis	**Result:** **LPF:** 1) Cut off frequency for Low pass filter: **Theoretical** | **Practical** $9\,KH_z$ | 2) Roll off rate: **Theoretical** | **Practical** 40dB/dec |

Copyright ©2017. cAAS. All rights reserved.

HPF: 1) Cut off frequency for HPF:

Theoretical	Practical
$4\,KH_z$	

2) Roll off rate:

Theoretical	Practical
40dB/dec	

12	Application Areas	Used in generation of high frequencies sinusoidal signal used in computer , instrumentation and in digital systems
13	Remarks	
14	Faculty Signature with Date	

.....

Experiment 05 : ADDER, INTEGRATOR AND DIFFERENTIATOR USING OP-AMP

-	**Experiment No.:**	5	**Marks**	10	**Date Planned**		**Date Conducted**	
1	Title	**ADDER, INTEGRATOR AND DIFFERENTIATOR USING OP-AMP**						
2	Course Outcomes	Design analog circuits using OPAMPs and 555 timerfor different applications						
3	Aim	To design adder, integrator and differentiator circuit for given specification using Op-Amp.						
4	Material / Equipment Required	1. IC 741 -Op-Amp 2. Resistors – as per the design 3. Capacitor – as per the design 4. Dc power supply 5. Signal generator 6. CRO 7. Digital multimeter/Voltmeter						
5	Theory, Formula, Principle, Concept	**Adder:** The most common application of Op-Amp is the summing-amplifier (or adder) circuit. Fig. 1 shows the inverting configuration of summing circuit with 2 inputs V_1 and V_2. Depending on the relationship between R_f, the feedback resistor and the input resistor R_1 and R_2, the circuit can be used as summing						

Copyright ©2017. cAAS. All rights reserved.

amplifier, scaling amplifier or averaging Amplifier. The input expression for the circuit can be written as (or obtained as)

$I_F = I_1 + I_2$

$\frac{-V_o}{R_f} = \frac{V_1}{R_1} + \frac{V_2}{R_2}$

$\therefore V_o = -\left[\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2\right]$ ..... (1)

- If $R_1 = R_2 = R_f = R$ in (1), then

  $V_o = -(V_1 + V_2)$ ---- summing amplifier. Here , the o/p voltage is equal to negative sum of all the inputs. Hence circuit act as summing amplifier.

- If R_1, R_2 R_f different , then the circuit is called scaling amplifier.

- If $R_1 = R_2 = R$ & if $\frac{R_f}{R} = \frac{1}{2}$, then the circuit can be used as an averaging circuit.

2. Integrator:

A circuit in which the output voltage is the integral of the input voltage is called integrator as shown in Fig2.

Relationship between voltage and current through capacitor is given by

$i_c = C \frac{dV_C}{dt}$

Applying Kirchhoff's law,

$i_1 \simeq i_f$

$\therefore \frac{V_{in}}{R_1} = C_F \frac{d(-V_O)}{dt}$

$\therefore V_O = -\frac{1}{R_1 C_F}\int_0^t V_{in}\,dt + \text{const}$

- As seen ,the o/p voltage is directly proportional to the negative of the input voltage and inversely proportional to time constant $R_1 C_F$.
- If V_{in} =0, then input offset voltage and the capacitor C_T produce error

Copyright ©2017. cAAS. All rights reserved.

voltage at output of integrator. To reduce the error voltages, resistor R_F is connected across the feedback capacitor C_F.

- Addition of R_F improves stability and low frequency roll off problems and hence minimizes the variations in the output voltage.
- The input signal will be integrated properly if the time period T of the signal is larger than or equal to $R_F \ C_F$.
- $\therefore T \geq R_F \ C_F$.

.

3. Differentiator:

Differentiator performs the mathematical operation of differentiation. The output voltage can be expressed in Fig. 3 as

$$i_c = i_F$$

$$\therefore C_1 . \frac{d(V_{in})}{dt} = - \frac{V_O}{R_F}$$

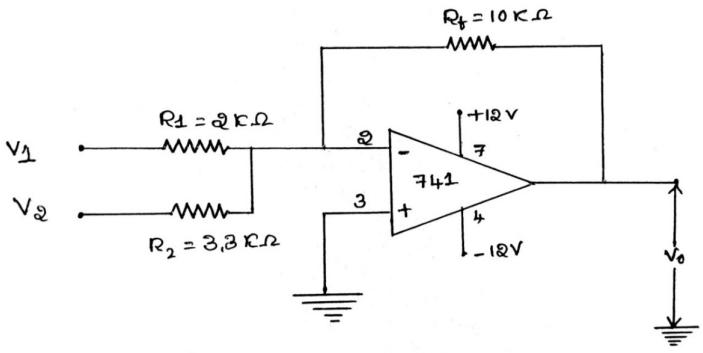
$$\therefore V_O = - R_F \ C_F \frac{d(V_{in})}{dt}$$

$\frac{R_F}{X_{C1}}$

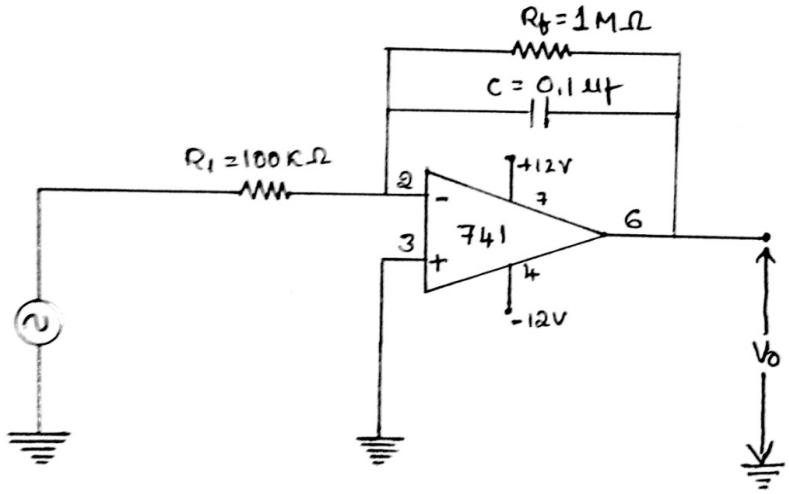
- The gain $\frac{R_F}{X_{C1}}$ increase with increase in frequency. Also, the input impedance X_{C1} decreases with increase in frequency which makes circuit susceptible to high frequency noise.
- The stability & high frequency noise problem can be corrected by two components C_F & R_1.
- The input signal will be differentiated properly if the time period T of the input signal is larger than or equal to $R_F \ C_1$.
- $\therefore T \geq R_F \ C_1$.

6	Procedure, Program, Activity, Algorithm, Pseudo Code	**Adder :** 1. Before wiring the circuit, check the components for its working . 2. Connect the circuit as shown in Fig.1. 3. Set the input voltages V_1 and V_2 and measure the output voltage V_o using multimeter. 4. Compare theoretical and practical output voltages

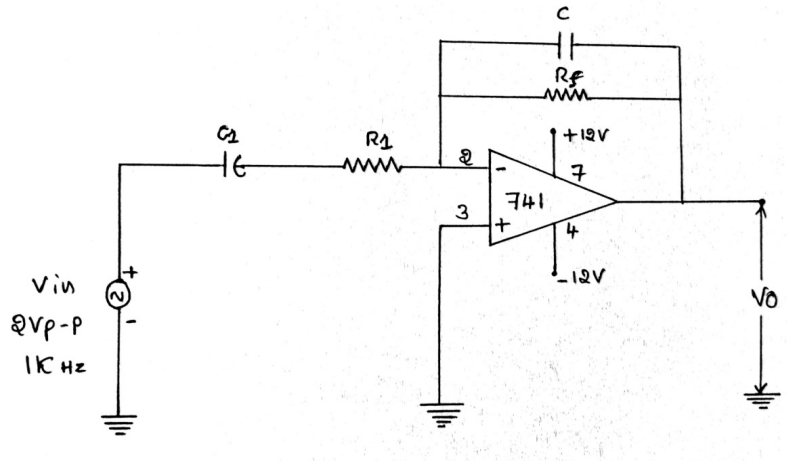
Copyright ©2017. cAAS. All rights reserved.

		5. Integrator Procedure: 6. Check all the components for its working. 7. Make the connections as shown in Fig.2. 8. Set the input voltage using signal generator to 4V (or 2V) peak to peak square wave at 1KHz frequency. 9. Observe the input & output signals of circuit on CRO. 10. Sketch the output for RC = 10T & RC =T & RC = 0.1T. Differentiator" 11. Check all the components for its working. 12. Make the circuit diagram as show in Fig.3. 13. Set the input voltage using signal generator to 4V (or 2V) peak to peak triangular wave at 1KHz frequency. 14. Sketch the output for RC= 10T, 0.025T & varying R. 15. Observe the output signal on CRO
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	Adder circuit  : Integrator:

Copyright ©2017. cAAS. All rights reserved.



Differentiator:



8 Observation Table, Look-up Table, Output

Input voltage (V)		Output voltage (V_o)	
V_1	V_2	**Theoretical** V_O	**Practical** V_O

9 Sample Calculations

ADDER Design:

Design a circuit to obtain the output voltage

$$V_O = -\left(5V_1 + 3V_2\right)$$

Solution:

Given $V_O = -\left(5V_1 + 3V_2\right)$

But $V_O = -\left[\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2\right]$

Copyright ©2017. cAAS. All rights reserved.

Given $\frac{R_f}{R_1}$ =5 & $\frac{R_f}{R_2}$ = 3

$\therefore R_f = 5R_1$, $R_f = 3R_2$

Choose R_f =10 KΩ

$\therefore R_1 = \frac{R_f}{5} = \frac{10k}{5}$ = 2KΩ ..... R_1 = 2KΩ

$R_2 = \frac{R_f}{3} = \frac{10k}{3}$ = 3.3KΩ ..... R_2 = 3.3KΩ

Integrator Design:

Given T = 1ms

a) Let RC =10T

Choose C=0.1μf

$\therefore$ R = $\frac{10T}{C} = \frac{10*1*10^{-3}}{0.1*10^{-6}}$

R =100kΩ

b) If RC = T

$\therefore$ R = $\frac{T}{C} = \frac{1*10^{-3}}{0.1*10^{-6}}$

$\therefore$ R =10KΩ

c) If RC =0.1 T

R = $\frac{0.1*1*10^{-3}}{0.1*10^{-6}}$

R = 1KΩ

Differentor Design:

Given T = 1ms

a) Let RC =10T

Choose C =0.1μf

$\therefore$ R = $\frac{10T}{C} = \frac{10*1*10-¿^{3}}{0.1*10^{-6}}¿$

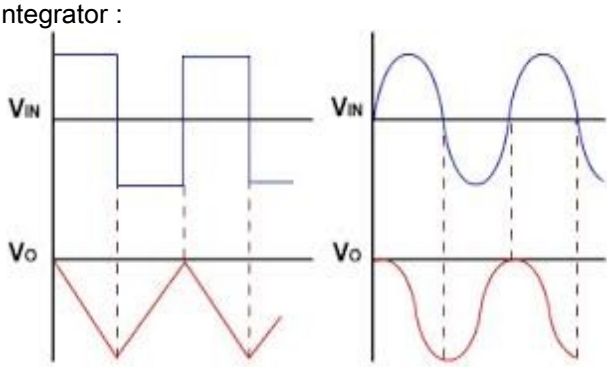
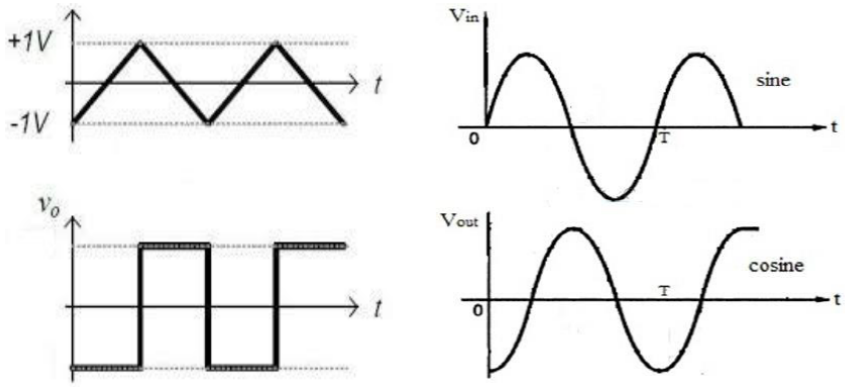
R = 100kΩ

b) If RC =0.025T

R = $\frac{0.025T}{C} = \frac{0.025*1*10^{-3}}{0.1*10^{-6}}$

R = 250Ω

Copyright ©2017. cAAS. All rights reserved.

		c) If RC =T R = $\frac{T}{C} = \frac{1*10^{-3}}{0.1*10^{-6}}$ R = 10KΩ
10	Graphs, Outputs	Integrator :  **Differentiator :** 
11	Results & Analysis	1.Adder: The obtained output voltage for inputs V_1 and V_2 are V_o =…….when V_1 =…… & V_2 =…….

Copyright ©2017. cAAS. All rights reserved.

		2. The operation of integrator circuit is verified. 3. Operation of differentiator circuit is verified.
12	Application Areas	The adder circuit is commonly used in 1). Analog computers 2). Audio mixers in which no of inputs are added or mixed to produce desired output. Integrator is commonly used in 1. Analog computers. 2. Analog to digital converter. 3. Signal wave shaping circuits Differentiator is commonly used in 1. Wave shaping circuits to detect high frequency component in input signal. 2. Rate of change detector in FM modulators.
13	Remarks	
14	Faculty Signature with Date	

Experiment 06 : SCHMITT TRIGGER

-	**Experiment No.:**	6	**Marks**	10	**Date Planned**		**Date Conducted**	
1	Title	**SCHMITT TRIGGER**						
2	Course Outcomes	Design analog circuits using OPAMPs and 555 timerfor different applications						
3	Aim	Design and Testing of Schmitt trigger circuit for different hysteresis value						
4	Material / Equipment Required	IC trainer, signal generator, CRO. Resisters, OP AMP, Patch Chords, Digital multimeter.						
5	Theory, Formula, Principle, Concept	A Schmitt trigger is a comparator circuit with hysteresis implemented by applying positive feedback to the non inverting input of a comparator or differential amplifier. It is an active circuit which converts an analog input signal to a digital output signal. In the non-inverting configuration, when the input is higher than a chosen threshold, the output is high. When the input is below a different (lower) chosen threshold the output is low, and when the input is between the two levels the output retains its value. This dual threshold action is called hysteresis and implies that the Schmitt trigger possesses memory and can act as a bistable multivibrator. Schmitt trigger devices are typically used in signal conditioning applications to remove noise from signals used in digital circuits, particularly mechanical contact bounce. They are also used in closed loop negative feedback configurations to						

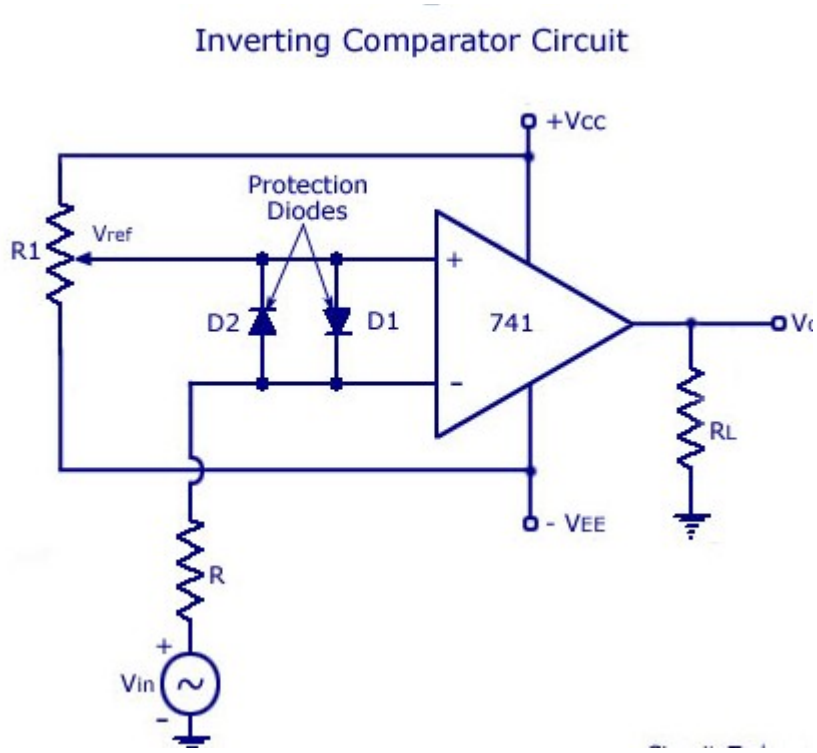
Copyright ©2017. cAAS. All rights reserved.

implement relaxation oscillators, used in function generators and switching power supplies.

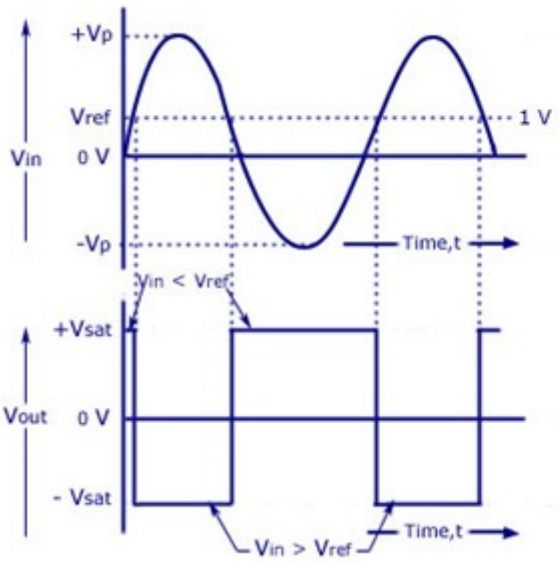
Test a Comparator circuit

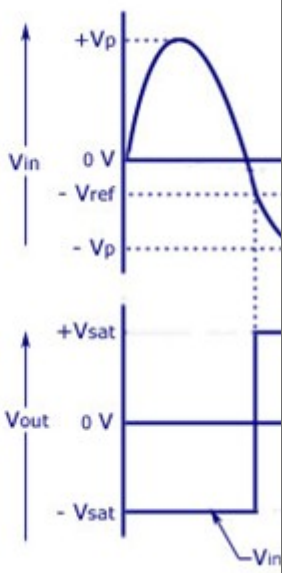
An inverting 741 IC op-amp comparator circuit is shown in the figure below. It is called an inverting comparator circuit as the sinusoidal input signal Vin is applied to the inverting terminal. The fixed reference voltage Vref is give to the non-inverting terminal (+) of the op-amp. A potentiometer is used as a voltage divider circuit to obtain the reference voltage in the non-inverting input terminal. Bothe ends of the POT are connected to the dc supply voltage +VCC and -VEE. The wiper is connected to the non-inverting input terminal. When the wiper is rotated to a value near +VCC, Vref becomes more positive, and when the wiper is rotated towards -VEE, the value of Vref becomes more negative. The waveforms are shown below.

Inverting Comparator circuit

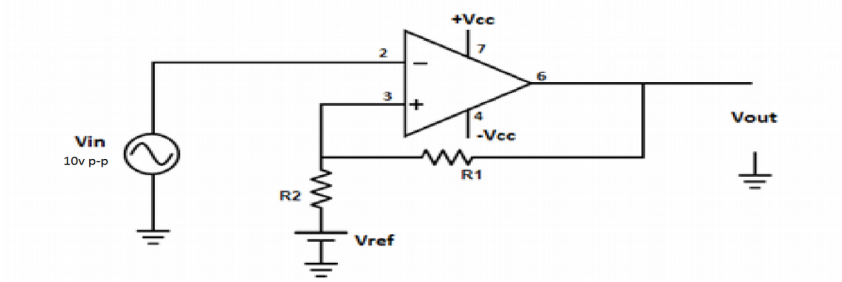


Copyright ©2017. cAAS. All rights reserved.

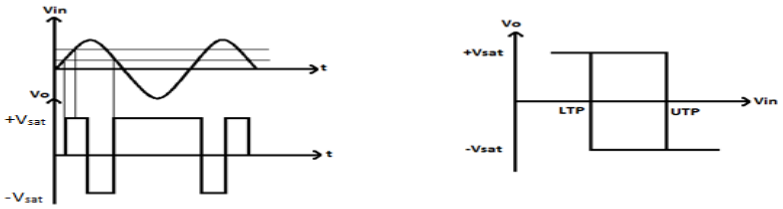




Input output waveforms for positive V_{ref} Input output waveforms for Negative V_{ref}

	Procedure, Program, Activity, Algorithm, Pseudo Code	Rig up the circuit as shown in figure 1. 1. Apply an input of 10V p-p, 1 kHz to the input terminals. 2. Observe the output waveform and measure the practical values of V_{UTP}, V_{LTP} in the x-y mode or the y-t mode. Also measure the value of V_{SAT}.
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	
8	Observation Table, Look-up Table, Output	
9	Sample Calculations	**Design: Formulae:** $V_{UTP} = V_{SAT} .R_2/ (R_1+R_2) +V_{REF}.R_1/ (R_1+R_2)$..... (1) $V_{LTP} = V_{SAT} (-R_2)/ (R_1+R_2) +V_{REF}. (R_1)/ (R_1+R_2)$ ..... (2) Adding (1) and (2) $V_{UTP} + V_{LTP} = V_{REF}\ 2R_1/ (R_1+R_2)$..... (3) $V_{UTP} – V_{LTP} = V_{SAT} =2R_2/ (R_1+R_2)$..... (4)

Copyright ©2017. cAAS. All rights reserved.

		V_{UTP} = 4V, V_{LTP} =2V, V_{SAT}=12V From (4) $R_2/(R_1+R_2)$ = 0.08333 Therefore R_1/R_2 =11 Choose R_2 =1 k ohm, R_1 = 11 k ohm From (3) $V_{REF} = (V_{UTP} + V_{LTP}).(R_1+R_2)/(2R_1)$, $V_{REF} = (6.12 \times 10^3)/(2.11 \times 10^3)$ V_{REF} = 3.272V
10	Graphs, Outputs	
11	Results & Analysis	V_{UTP} (Practical) = ……..Volts. V_{LTP} (Practical) = ……..Volts. V_{+sat} =……..Volts. V_{-sat} =……..Volts.
12	Application Areas	Used in signal conditioning to remove noise
13	Remarks	
14	Faculty Signature with Date	

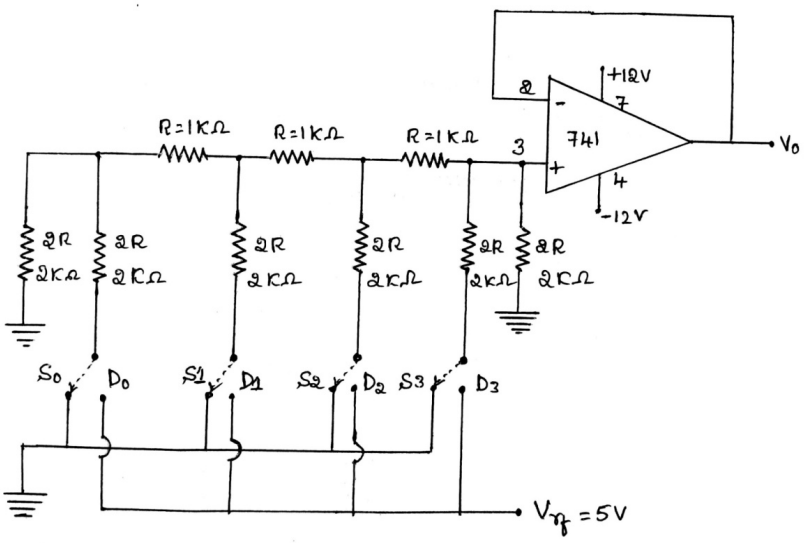
Experiment 07 : R-2R DAC USING OP-AMP

-	Experiment No.:	8	Marks	10	Date Planned		Date Conducted	
1	Title	**R-2R DAC USING OP-AMP**						
2	Course Outcomes	Design analog circuits using OPAMPs and 555 timerfor different applications						
3	Aim	.1. To design 4 bit R-2R digital to analog convertor using Op-Amp and verify its operation using input toggle switch. 2. To generate staircase waveform using mod-16 counter.						
4	Material / Equipment Required	**Components Required:** 1. IC 741 Op-Amp 2. Resistors –As per the design 3. Dc power supply 4. IC trainer kit						

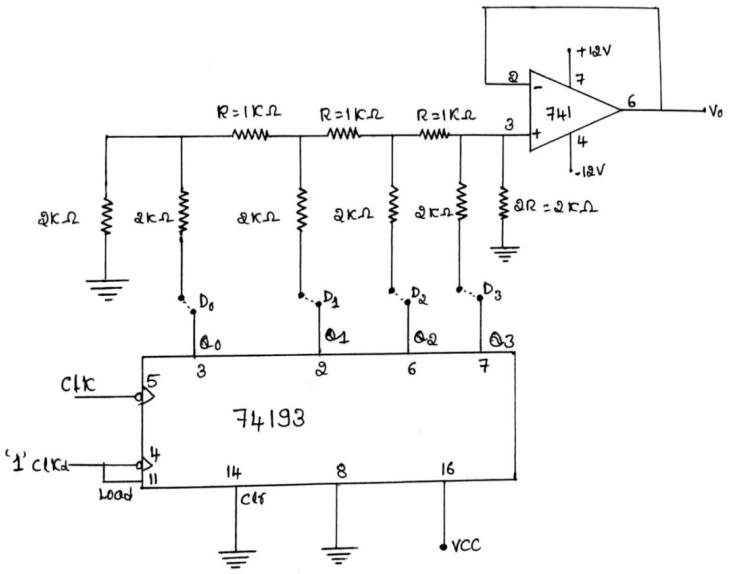
Copyright ©2017. cAAS. All rights reserved.

		5. CRO 6. Millimeter / Voltmeter 7. IC7493 or equivalent
5	Theory, Formula, Principle, Concept	R-2R DAC is shown in Fig. 1. It consists of only two resistors R and 2R forming ladder network and an Op-Amp acting as voltage follower. Here D_o, D_1, D_2 & D_3 are digital inputs which are controlled by the Switches S_0, S_1, S_2, & S_3. When the digital input is '1', then the corresponding switch connects the resistor 2R to V_{ref} and when digital input is '0', then the switch connects the resistor 2R to the ground line. Since the ladder is composed of linear resistors, it is a linear network and hence principle of superposition can be used to obtain the output voltage. • The analog output voltage V_o for 4 bit DAC can be written as $V_o = [2^3 D_3 + 2^2 D_2 + 2^1 D_1 + 2^0 D_0 + ¿¿] V_1$ where $V_1 = [\frac{V_{\text{ref}}}{2^N}] * [\frac{2R}{R+2R}] = \frac{V_{\text{ref}}}{2^N} [\frac{2R}{3R}] = \frac{V_{\text{ref}}}{2^N} [\frac{2}{3}]$ Since N=4 [4 bit DAC], V_1 becomes $V_1 = \frac{V_{\text{ref}}}{2^4} * \frac{2}{3}$ $V_1 = \frac{V_{\text{ref}}}{24}$ $\therefore V_o = [8D_3 + 4D_2 + 2D_1 + D_0] * \frac{V_{\text{ref}}}{24}$
6	Procedure, Program, Activity, Algorithm, Pseudo Code	1. Verify the components for its working. 2. Make the connection as shown in Fig.1. 3. For different digital inputs, measure the output voltage using multimeter. 4 Verify whether the theoretical values is matching with practical values & plot the graph of input V/s output. **Procedure:** 1. Check the components for its working. 2. Make connection as shown in Fig. 3. 3. Construct modulo16 counter using suitable IC like 7493 or 74193.

Copyright ©2017. cAAS. All rights reserved.

		4. Apply clock (Say 1KHz or 10KHz) and observe staircase waveform on CRO. 5. Find resolution and sketch input and output waveform on graph sheet.
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	**R-2R ladder Network:** **a). circuit diagram:**  1. To generate staircase waveform using DAC circuit & mod-16 counter **Circuit diagram:**

Copyright ©2017. cAAS. All rights reserved.



8 Observation Table, Look-up Table, Output

Tabular column:

Digital inputs				Decimal equivalent	Analog output voltage
D_3	D_2	D_1	D_0		Theoretical V_0 (V)
0	0	0	0	0	0
0	0	0	1	1	0.20833
0	0	1	0	2	0.4166
0	0	1	1	3	0.625
0	1	0	0	4	0.833
0	1	0	1	5	1.00416
0	1	1	0	6	1.25
0	1	1	1	7	1.45
1	0	0	0	8	1.66
1	0	0	1	9	1.875
1	0	1	0	10	2.05
1	0	1	1	11	2.29
1	1	0	0	12	2.50
1	1	0	1	13	2.708
1	1	1	0	14	2.916
1	1	1	1	15	3.125

Tabular Column:

Copyright ©2017. cAAS. All rights reserved.

		Step width / Resolution

Step width		Resolution	
Ideal	Obtained	Ideal	Obtained

$$\% \text{ Resolution} = \frac{\text{Stepsize}}{\text{Full scale}} * 100$$

$$= \frac{\text{Stepwidth}}{4} * 100$$

9	Sample Calculations	**Given: No of steps =15**

Solution:

w.k.t, No of steps = $2^N - 1$

$15 = 2^N - 1$

$14 = 2^N$

Apply $\log_2$ on both sides

$\log_2 14 = \log_2 2^N$

$\log_2 14 = N$

$$\frac{\log 14}{\log 2} = N$$

$N = 3.8$

∴ Resolution = N

Use 4 bit DAC with minimum step size as 0.208V.

This is a 4 bit R-2R ladder N/W shown in Fig3.

a) Given :N=4 and step size =0.5V

Solution:

Minimum step size = $\frac{V_{ref}}{24} = \frac{5}{24}$ = 0.208V

Given step = 0.5V

∴ Maximum o/p voltage = V_{omax} = step size * No of steps

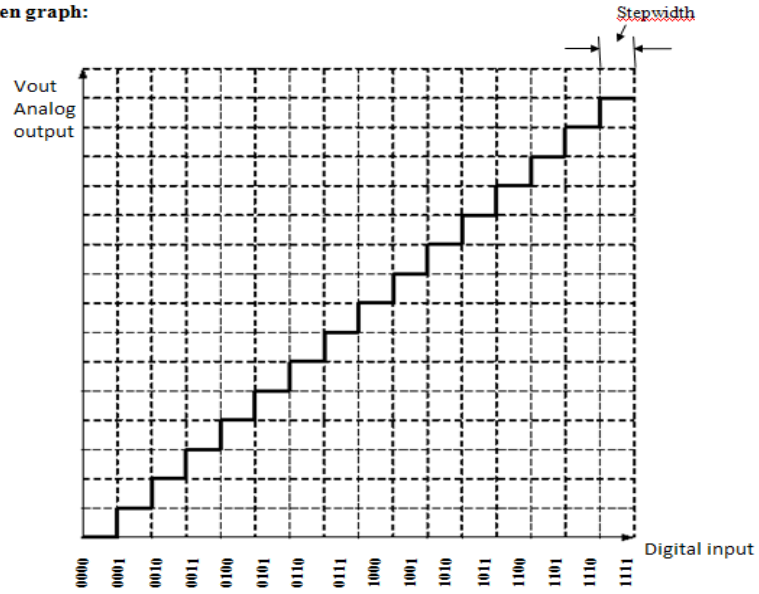
= 0.5 * (2^4 -1)

= 0.5 * 15

= 7.5V

Given steps =0.5

Copyright ©2017. cAAS. All rights reserved.

		$\therefore$ Gain = $A_f = \frac{\text{Given step}}{\text{minimum step}} = \frac{0.5}{0.208}$ = 2.4V But $A_f = 1+\frac{R_f}{R_1}$ $2.4 = 1+\frac{R_f}{R_1}$ $\therefore \frac{R_f}{R_1} = 1.4$ $\therefore R_f = 1.4\, R_1$ Let R_1 =10KΩ $\therefore R_f$ =1.4*10KΩ = 14KΩ $R_f \approx$15KΩ
10	Graphs, Outputs	**Specimen graph:** 
11	Results & Analysis	1.The obtained resolution of DAC is …… 2. Working of R-2R DAC is verified.
12	Application Areas	Typical applications for D/A converter include microcomputer interfacing, CRT graphics generations, programmable power supplies, digitally controlled gain circuits, digital filters, etc,.
13	Remarks	
14	Faculty Signature with Date	

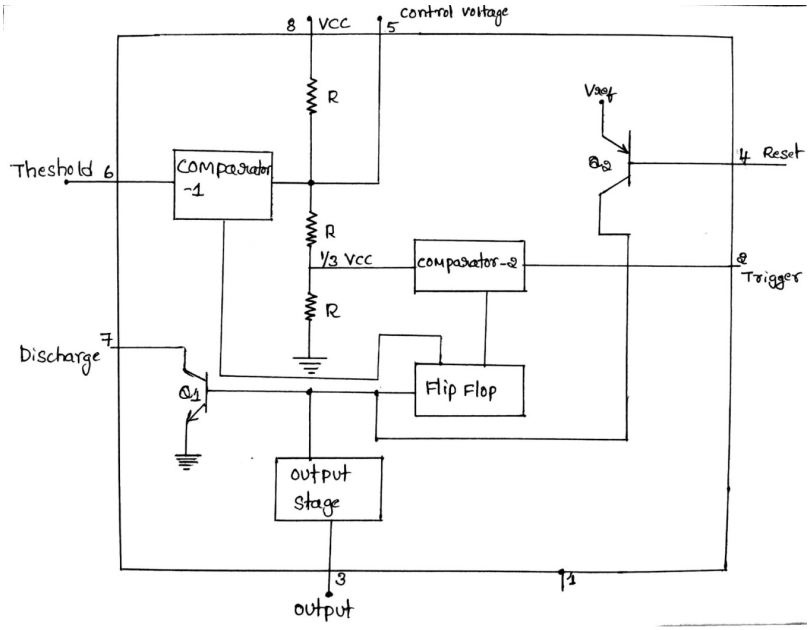
Copyright ©2017. cAAS. All rights reserved.

Experiment 08 : ASTABLE AND MONOSTABLE MULTIVIBRATOR USING IC 555

-	Experiment No.:	8	Marks	10	Date Planned		Date Conducted	
1	Title	**ASTABLE AND MONOSTABLE MULTIVIBRATOR USING IC 555**						
2	Course Outcomes	Design analog circuits using OPAMPs and 555 timerfor different applications						
3	Aim	1.Design Astable multi-vibrator using IC 555 timer to generator a clock frequency of 1KHz with 0.75 duty cycle (unsymmetrical) and 0.5 duty cycle (symmetrical). 2. Design monostable multi-vibrator using IC 555 timer.						
4	Material / Equipment Required	1. 555timer 2. Resistors – As per the design 3. Capacitors – As per the design 4. Power supply 5. Diode – 1N4001 6. Signal generator						
5	Theory, Formula, Principle, Concept	**Astable multivibrator:** An astable multi-vibrator, often called a free running multi-vibrator is a rectangular wave generating circuit. The circuit does not require any external trigger to change the output & hence the name free running. The time during which the output is either high or low is determined by the two resistors & capacitors which are connected externally. Fig.1 shows the 555 timer connected as an astable multivibrator. To understand the circuit operations consider the internal block diagram of the 555 timer. Initially when output is high, capacitor C starts towards V_{CC} through R_A and R_B. However, as soon as voltage across the capacitor equals $\frac{2}{3}$ V_{CC}, comparator -1 triggers the flip-flop and the o/p switches low. Now capacitor C starts discharging through R_B and transistor Q_1. When the voltage across C equals $\frac{1}{3}$ V_{CC}, comparators output triggers the flip-flop and output goes to high. Then the cycle repeats the output voltage and						

Copyright ©2017. cAAS. All rights reserved.

capacitor voltage waveform as shown in Fig. 2.



The time during which the capacitor charges from $\frac{1}{3}\ V_{CC}$ to $\frac{2}{3}\ V_{CC}$ is equal to the time the output is high & is given by

$$t_C = 0.69(R_A + R_B) C$$

The time during which, the capacitor discharges from $\frac{2}{3}\ V_{CC}$ to $\frac{1}{3}\ V_{CC}$ is equal to the time the output is low & is given by

$$t_d = 0.69(R_B) C$$

∴ Total period $T = t_C + t_d$

$$= 0.69(R_A + R_B) C$$

Hence frequency of oscillator is $f_o = \frac{1}{T} = \frac{1.45}{(R_A+2R_B)C}$

The duty cycle is the ratio of time t_C during which the output is high to the total period T.

$$\% \text{ duty cycle} = \frac{t_C}{T} * 100$$

$$= \frac{R_A+R_B}{R_A+2R_B} * 100\%$$

As seen from above equation, astable multi-vibrator will not produce square wave unless the resistance R_A =0. With R_A =0, pin 7 is directly connected to

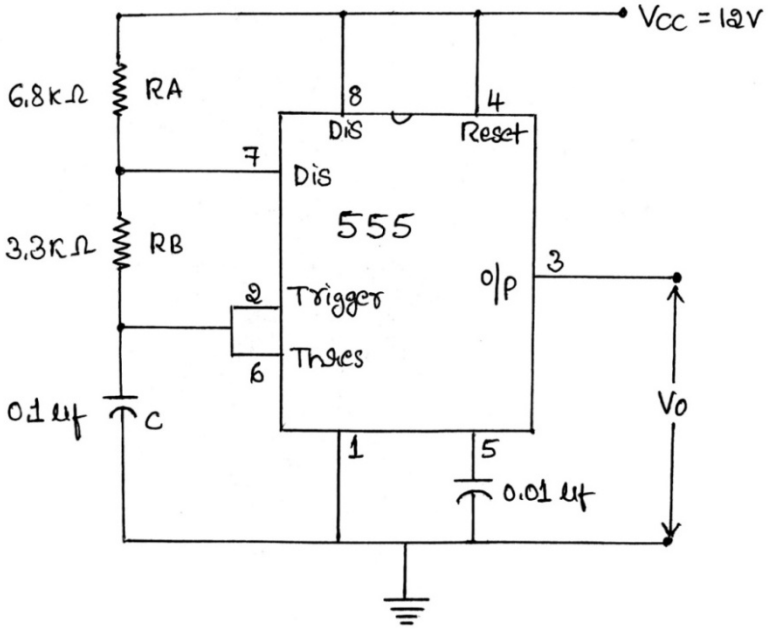
Copyright ©2017. cAAS. All rights reserved.

		V_{CC} & when capacitor discharge through R_B , an extra current is supplied to Q_1 by V_{CC} through short between 7 & V_{CC} which damages Q_1 & hence timer. Without reducing R_A to 0Ω, the astable multi-vibrator can produce square wave output simply by connecting diode across R_B as shown in Fig.3. **2. Monostable multivibrator:** A monostable multi-vibrator is often called as one shot multi-vibrator. It is a pulse generating circuit in which the duration of the pulse is determined by the RC network connected externally. When an external trigger pulse is applied, the output is forced to go high. The time the output remains high is determined by the external RC network connected to the timer. At the end of time interval, the output automatically reverse back to its logic low stable states. The output stays low until the trigger pulse is again applied. Then the cycle repeats. The monostable circuit has only one stable state & hence the name monostable. **Circuit operation:** The circuit is shown in Fig. 5. Initially, when the output is low, transistor Q_1 is on & capacitor C is shorted to ground. However, upon the application of negative trigger pulse to pin 2, transistor Q_1 is turned off, which releases the short circuit across the external capacitor C & drives the output high.The capacitor C now starts charging up towards V_{CC} through R_A . However,when the voltage across the capacitor equals $\frac{2}{3}$ V_{CC} , comparator 1 output switch from low to high which in turn dives the output to its low state via the flip-flop. The output of flip-flop turns Q_1 ON & hence capacitor C rapidly discharges through the transistor. The output remains low until a trigger pulse is applied again. The time during which the output remains high is given by t_p = 0.69 R_A C
6	Procedure, Program, Activity, Algorithm, Pseudo Code	**Procedure:** **Astable multi-vibrator:** **i. D>50%** 1. Verify the components for its working.

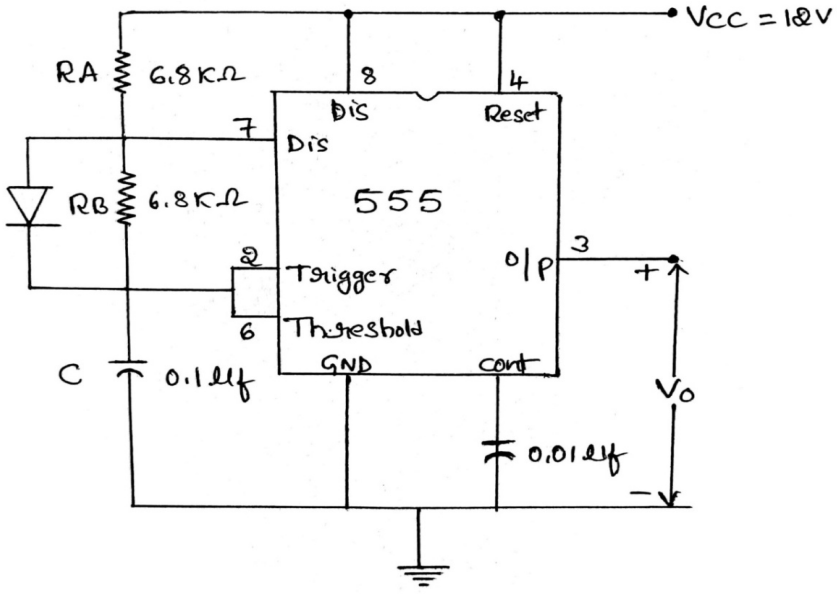
Copyright ©2017. cAAS. All rights reserved.

		2. Connect the Astable multi-vibrator circuit as shown in Fig.1. 3. Switch the DC power supply (V_{CC} = 12V) and observe the output waveform. On CRO at pin 3. 4. Measure the output pulse amplitude. 5. Observe capacitor voltage waveform at pin 6 & measure the maximum & minimum levels (V_{UT} & V_{LT}). 6. Calculate duty cycle'd' & output frequency f & verify with theoretical values. **ii) For D ≤¿¿ 50%** 1. Connect the circuit as shown in Fig. 3. 2. Set R_A = R_B = R [For 50% duty cycle]. 3. Select suitable value for C. 4. Measure output voltage & note capacitor voltage on CRO & measure V_{UT} , V_{LT} . 5. Calculate d & output frequency f. **Monostable multi-vibrator:** 1. Check the components for its working. 2. Connect the circuit as shown in Fig. 5. 3. Switch power supply ON & apply periodic input trigger pulse [negative going trigger] at pin 2 using pulse generator (or signal generator). 4. Adjust input frequency of pulse generator to 80Hz & adjust the input pulse amplitude to 12V. 5. Observe timer output at pin 3 on CRO & calculate f. **NOTE:** If T = 1 ms, then f = 1KHz, Set input freq ¿ 1KHz say 800/500Hz If T =10 MS , then f = 100Hz , Set input freq ¿ 100Hz say 80Hz
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	**1. Astable multivibrator** **Circuit diagram:** **I. Un- symmetrical Astable multivibrator:**

Copyright ©2017. cAAS. All rights reserved.



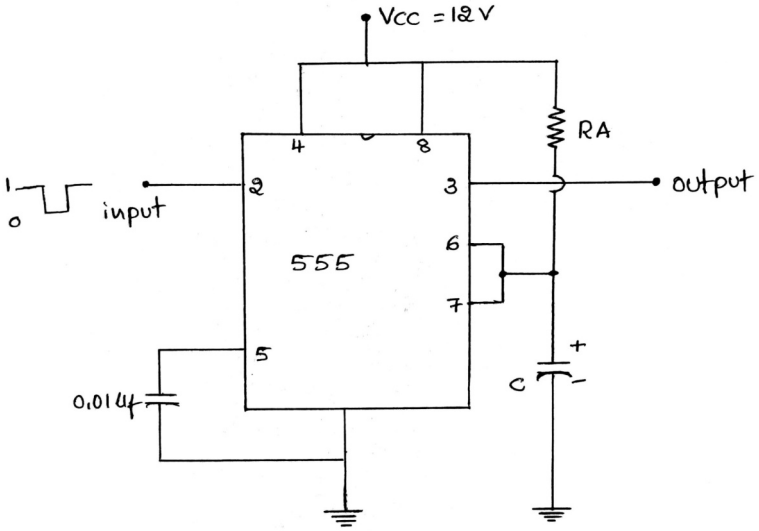
II. Symmetrical Astable multivibrator:



Monostable multivibrator:

Circuit diagram:

Copyright ©2017. cAAS. All rights reserved.



8 Observation Table, Look-up Table, Output

V_{UT} (V)		V_{LT} (V)		T_H (mS)		T_L (mS)		T(mS)
Theoretical =2/3 V_{CC}	Practical	Theoretical =1/3 V_{CC}	Practical	Theoretical	Practical	Theoretical	Practical	Theoretical

monostable multivibrator

T(ms)		2/3 V_{CC} (V)	
Theoretical	Practical	Theoretical	Practical

9 Sample Calculations

Design:

Design Astable multi-vibrator to produce 1KHz square wave with duty cycle of 75%.

Solution:

Given duty cycle, D=0.75, f = 1 KHz

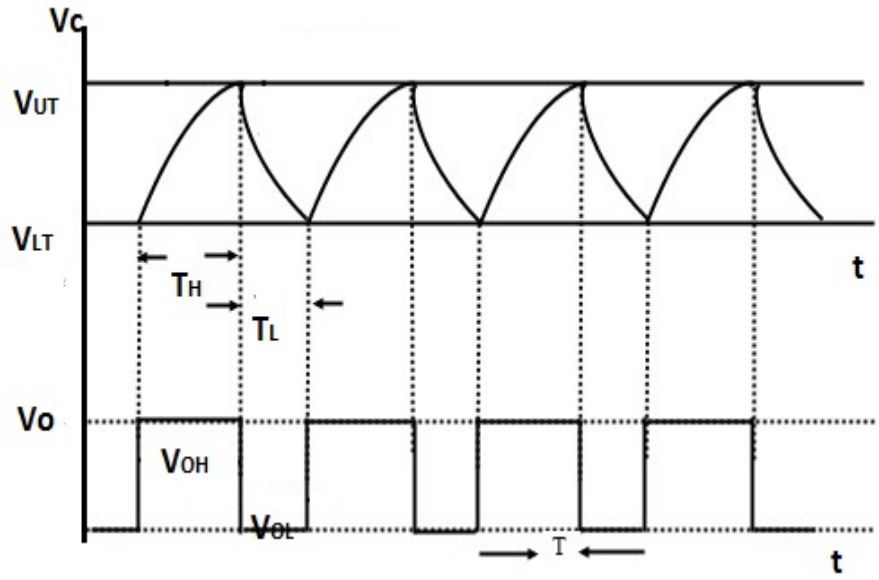
Time period T= $\frac{1}{f} = \frac{1}{1\,\text{KHz}}$ =1ms

But T = $T_H + T_L$

Copyright ©2017. cAAS. All rights reserved.

		∴ 1ms = T_H+ T_L ……(1) Duty cycle, D = $\frac{T_H}{T}$ 0.75 = $\frac{T_H}{T}$ ……. T_H = 0.75 T_H = 0.75(1ms) T_H = 0.75ms ……(2) Substitute Eq. (2) in Eq. (1) gives ∴ T_L = T- T_H =1m – 0.75m T_L = 0.25ms But T_L = 0.69 R_B C Let C =0.1μF ∴ T_L = 0.69* R_B *0.1μ ∴ R_B = $\frac{T_L}{0.69*0.1\mu}$ = $\frac{0.25m}{0.69*0.1\mu}$ =3.6KΩ R_B = 3.6KΩ But T_H = 0.69(R_A + R_B) C 0.75μf = 0.69(R_A + R_B) 0.1μ R_A + R_B = 10.82K ∴ R_A = 10.82K - R_B = 7.2KΩ ∴ Select R_A =6.8KΩ & R_B =3.3KΩ **Design monostable multi-vibrator having time delay t_p =10ms** **Solution:** Given t_p =10ms Choose C =0.1μf ∴ R_A = $\frac{t_p}{1.1C}$ = $\frac{10*10^{-3}}{1.1*0.1*10^{-6}}$ =90KΩ ∴ Select R_A =100 KΩ
10	Graphs, Outputs	

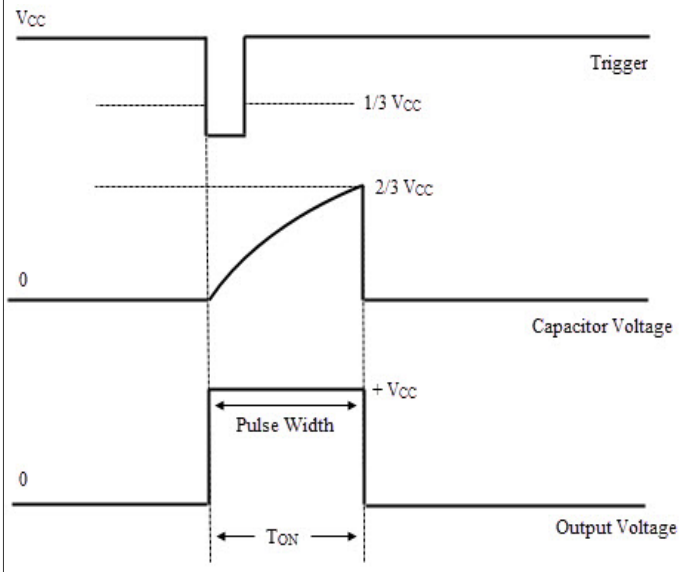
Copyright ©2017. cAAS. All rights reserved.



$V_{UT} = \frac{2}{3} V_{CC}$, V_{LT} = 1/3 V_{CC}

Note: For symmetrical astable multi-vibrator $V_{OH} = V_{OL}$

Monostable multi-vibrator



11	Results & Analysis	1. Unsymmetrical Astable multivibrator was designed and verified with % duty cycle =…… 2 symmetrical Astable multivibrator was designed and verified 3. Operation of monostable multi-vibrator is verified.
12	Application Areas	**Astable multivibrator:** 1. Square wave oscillator.

Copyright ©2017. cAAS. All rights reserved.

		2 Free running ramp generator. **Manostable multivibrator:** 1. Frequency divider. 2. Pulse stretcher.
13	Remarks	
14	Faculty Signature with Date	

Experiment 09 : RC PHASE SHIFT OSCILLATOR AND HARTLEY OSCILLATOR

-	**Experiment No.:**	9	**Marks**	10	**Date Planned**		**Date Conducted**	
1	Title	RC Phase shift oscillator and Hartley oscillator						
2	Course Outcomes	Simulate and analyze analog circuits that uses transistor and ICs for different electronic applications.						
3	Aim	To design and test the following tuned oscillator circuits for the given frequency. (a) RC Phase Shift Oscillator using BJT. (b) Hartley Oscillator using BJT.						
4	Material / Equipment Required							

Sl.No.	Particulars	Specification	Quantity
1	Transistor	SL100	
2	Resistor	1.2KΩ	1
		1.8K Ω	2
		4.7K Ω	3
		12K Ω	1
		62K Ω	1
3	DRB	10K Ω	1
4	Capacitor	0.47µf	2
		0.01µf	3
		4.7µf	1
5	DCB		1
6	VRPS	0 – 32 V	2
7	CRO	20 MHz, Dual Channel	1
8	CRO Probes		3
9	Digital Multimeter		1

Copyright ©2017. cAAS. All rights reserved.

Hartley Oscillator using BJT.

Sl.No.	Particulars	Specification	Quantity
1	BJT		2
2	capacitors Resistor	0.1µf	2
		4.7µf	1
		8.84nF	1
		330Ω	1
		820 Ω	1
3		2M Ω	1
4	Inductors CRO	240µH	1
		100µH	1
		Dual Channel	1

5 Theory, Formula, Principle, Concept

RC PHASE SHIFT:

An oscillator is an electronic circuit for generating an AC signal voltage with a DC supply as the

Only input requirement. The frequency of the generated signal is decided by the circuit elements used. An oscillator requires an amplifier, a frequency selective network and a positive feedback from the output to the input. The Barkhausen criterion for sustained oscillation is Aβ = 1 where A is the gain ofthe amplifier and β is the feedback factor (gain).The unity gain means signal is in phase. (If the signal is1800 out of phase and gain will be -1). RC-Phase shift Oscillator has a CE amplifier followed by three sections of RC phase shift feed-back Networks. The output of the last stage is return to the input of the amplifier. The values of R and C are chosen such that the phase shift of each RC section is 60º.Thus The RC ladder network produces a total phase shift of 180º between its input and output voltage for the given frequency. Since CE Amplifier produces 180º phases shift. The total phase shift from the base of the transistor around the circuit and back to the base will be exactly 360º or 0º. This satisfies the Barkhausen condition for sustaining oscillations and total loop gain of this circuit is greater than or equal to 1, this condition used to generate the sinusoidal oscillations

HARTLEY:

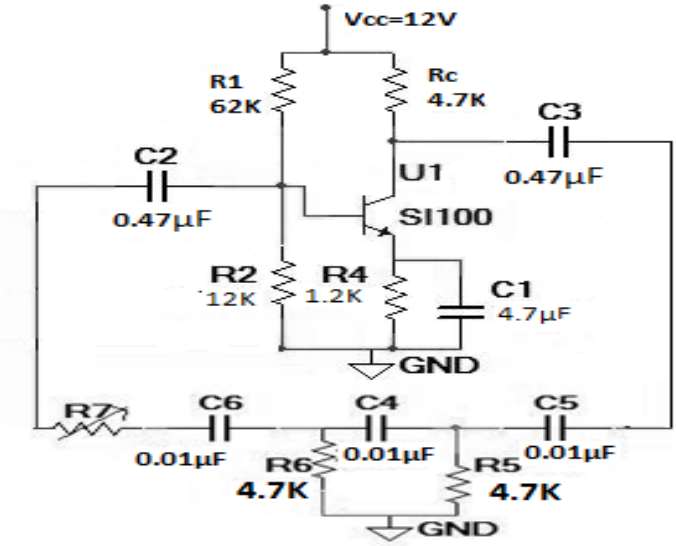
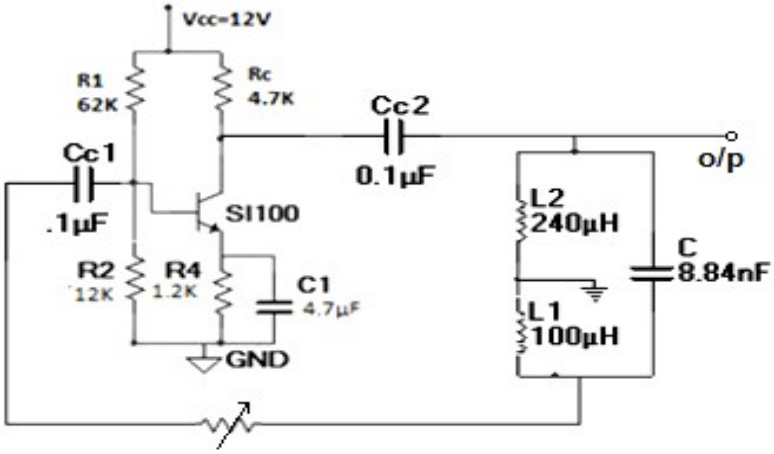
An oscillator is an electronic circuit for generating an AC signal voltage with a DC supply as the

Only input requirement. The frequency of the generated signal is decided by the circuit elements used. An oscillator requires an amplifier, a frequency selective network and a positive feedback from the output to the input. The Barkhausen criterion for sustained oscillation is Aβ = 1 where A is the gain ofthe amplifier and β is the feedback factor (gain).The unity gain means signal is in phase The Hartley oscillator is an electronic oscillator circuit in which the oscillation frequency is determined by a tuned circuit consisting of capacitors and inductors, that is, an LC oscillator. The Hartley oscillator is distinguished by a tank circuit consisting of two series-connected coils (or, often, a tapped coil) in parallel with a capacitor, with an amplifier between the relatively high impedance across the entire LC tank and the

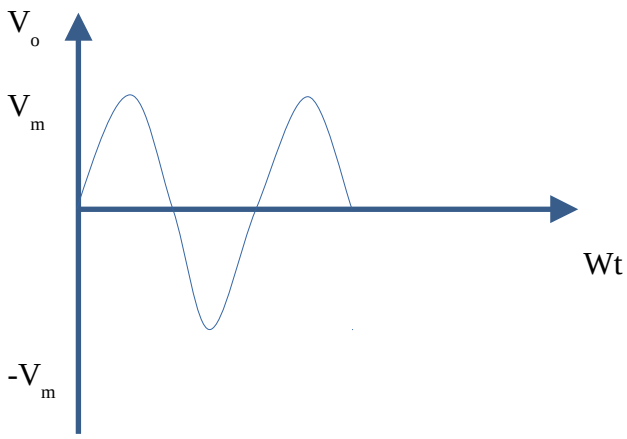
Copyright ©2017. cAAS. All rights reserved.

		relatively low voltage/high current point between the coils. The Hartley oscillator is the dual of the Colpitts oscillator which uses a voltage divider made of two capacitors rather than two inductors. Although there is no requirement for there to be mutual coupling between the two coil segments, the circuit is usually implemented using a tapped coil, with the feedback taken from the tap, as shown here. The optimal tapping point (or ratio of coil inductances) depends on the amplifying device used, which may be a bipolar junction transistor.
6	Procedure, Program, Activity, Algorithm, Pseudo Code	1. Rig up the circuit as shown in figure 2. place all the required components from multi-sim library 3. click on run button and observe the out put ***To plot frequency response*** 1. Place the components in Multisim. 2. Rig up the circuit as shown in circuit diagram. 3. Click on the run button and Double click on Oscilloscope. 4. Observe the output waveforms on Oscilloscope. 5. Measure frequency of the output signal, compare it with theoretical frequency. HARTLEY: ***6. To plot frequency response*** 7. Place the components in Multisim. 8. Rig up the circuit as shown in circuit diagram. 9. Click on the run button and Double click on Oscilloscope. 10. Observe the output waveforms on Oscilloscope. 11. Measure frequency of the output signal, compare it with theoretical frequency.

Copyright ©2017. cAAS. All rights reserved.

7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	 HARTLEY  :
8	Observation Table, Look-up Table, Output	
9	Sample Calculations	
10	Graphs, Outputs	

Copyright ©2017. cAAS. All rights reserved.

		
11	Results & Analysis	The RC Phase Shift Oscillator and Hartley simulated and output is verified
12	Application Areas	RC phase shift oscillator is used in musical instrument, GPS unit and in voice synthesis Hartley oscillator are used in radio receivers
13	Remarks	
14	Faculty Signature with Date	

Experiment 10 : NARROW BAND-PASS FILTER AND NARROW BAND-REJECT FILTER

-	**Experiment No.:**	10	**Marks**	10	**Date Planned**		**Date Conducted**	
1	Title	Narrow Band-pass Filter and Narrow band-reject filter						
2	Course Outcomes	Simulate and analyze analog circuits that uses transistor and ICs for different electronic applications.						
3	Aim	To simulate and analyze the Narrow Band-pass Filter and Narrow band-reject filter						
4	Material / Equipment Required							
5	Theory, Formula, Principle, Concept	A narrow bandpass filter employing multiple feedback is depicted in figure. This filter employs only one op-amp, as shown in the figure. In comparison to all the filters discussed so far, this filter has some unique features that are given below. **1. It has two feedback paths, and this is the reason that it is called a multiple-feedback filter.** **2. The op-amp is used in the inverting mode.**						

Copyright ©2017. cAAS. All rights reserved.

The frequency response of a narrow bandpass filter is shown in fig(b).

Generally, the narrow bandpass filter is designed for specific values of centre frequency f_c and Q or f_c and BW. The circuit components are determined from the following relationships. For simplification of design calculations each of **C_1 and C_2 may be taken equal to C.**

$R_1 = Q/2\Pi f_c C A_f$

$R_2 = Q/2\Pi f_c C(2Q^2 - A_f)$

and $R_3 = Q / \Pi f_c C$

where A_f, is the gain at centre frequency and is given as

$A_f = R_3 / 2R_1$

The gain A_f however must satisfy the condition $A_f < 2 Q^2$.

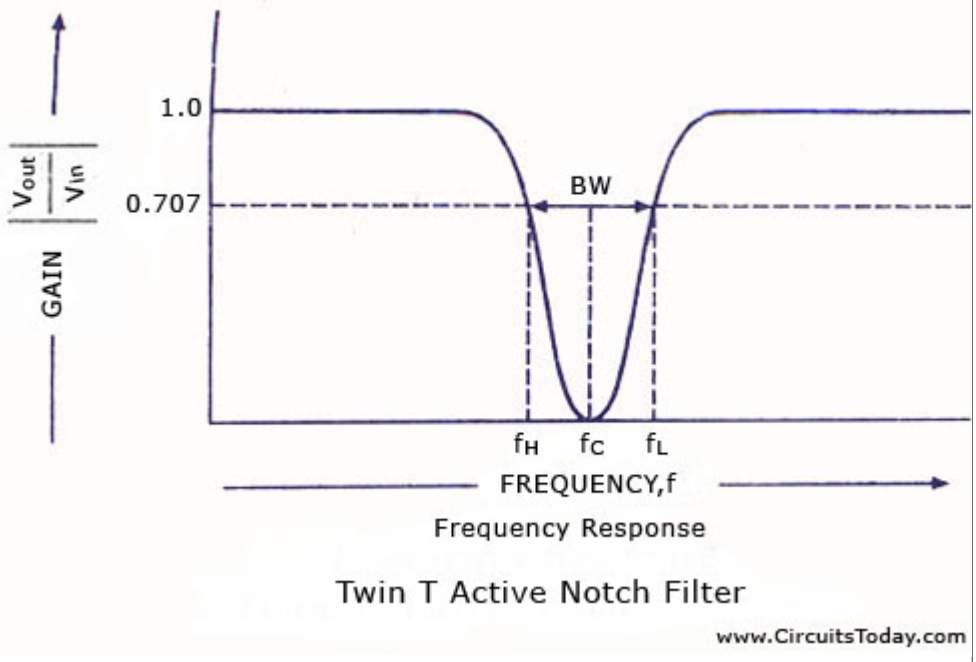
The centre frequency f_c of the multiple feedback filter can be changed to a new frequency f_c' without changing, the gain or bandwidth. This is achieved simply by changing R_2 to R'_2 so that

$R'_2 = R_2 [f_c/f'_c]^2$

BAND REJECT FILTER:

This is also called a notch filter. It is commonly used for attenuation of a single frequency such as 60 Hz power line frequency hum. The most widely used notch filter is the twin-T network illustrated in fig. (a). This is a passive filter composed of two T-shaped networks. One T-network is made up of two resistors and a capacitor, while the other is made of two capacitors and a resistor.One drawback *of* above notch filter (passive twin-T network) is that it has relatively low figure of merit Q. However, Q of the network can be increased significantly if it is used with the voltage follower, as illustrated in fig. (a). Here the output of the voltage follower is supplied back to the junction of R/2 and 2 C. The frequency response of the active notch filter is shown in fig *(b).*

Copyright ©2017. cAAS. All rights reserved.



Notch filters are most commonly used in communications and biomedical instruments for eliminating the undesired frequencies.

A mathematical analysis of this circuit shows that it acts as a lead-lag circuit with a phase angle, shown in fig. (b). Again, there is a frequency f_c at which the phase shift is equal to 0°. In fig. (c), the voltage gain is equal to 1 at low and high frequencies. In between, there is a frequency f_c at which voltage gain drops to zero. Thus such a filter notches out, or blocks frequencies near f_c. The frequency at which maximum attenuation occurs is called the notch-out frequency given by

$f_n = F_c = 2\prod RC$

Notice that two upper capacitors are C while the capacitor in the centre of the network is 2 C. Similarly, the two lower resistors are R but the resistor in the centre of the network is 1/2 R. This relationship must always be maintained.

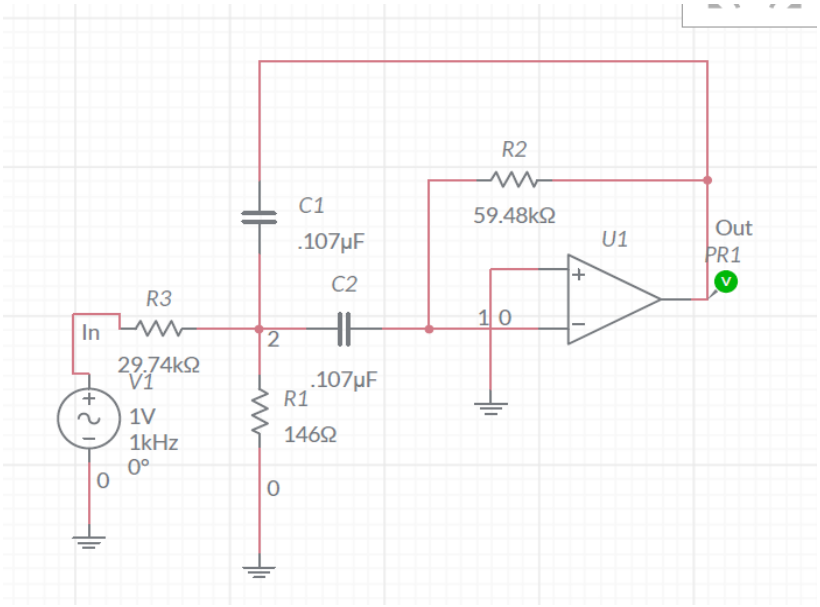
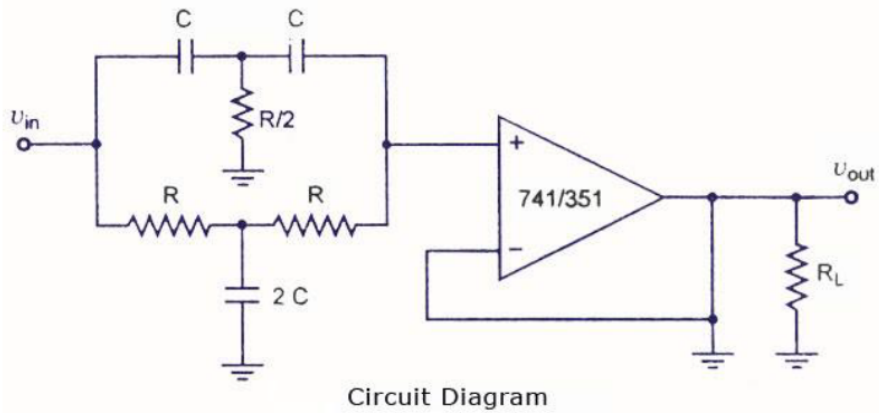
Let us consider the narrow band notch filter circuit. We know that the notch filter is used to eliminate single frequency. Thus let us consider the frequency to eliminate be 120 Hz. The capacitor value C= 0.33 μF.

By using the centre frequency $f_C = 1/(2\pi RC)$

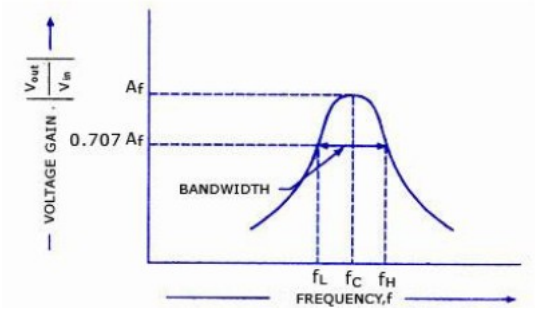
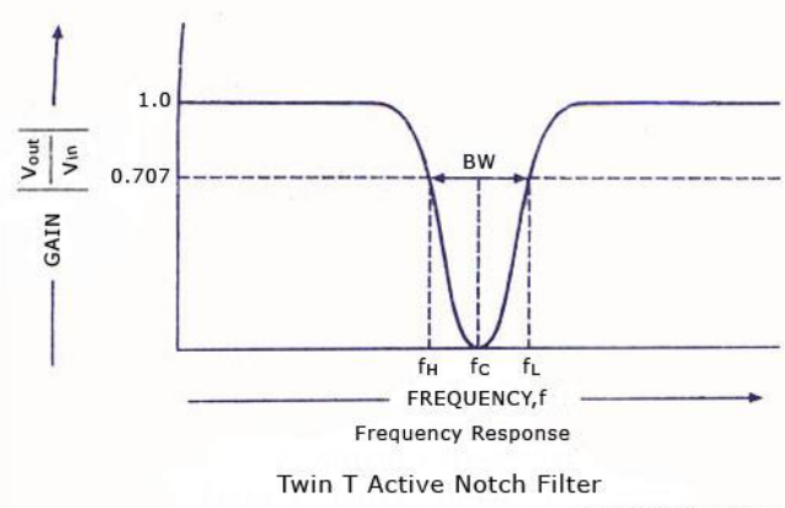
$$R = 1/(2\pi f_C C) = 1 / (2\pi x120 \times 0.33 \times 10^{-6}) = 4\ k\Omega$$

Thus, in order design the notch filter to eliminate 120 Hz frequency we have to take two parallel resistors with 4 kΩ each and the two capacitors in parallel with 0.33 μF each.

Copyright ©2017. cAAS. All rights reserved.

6	Procedure, Program, Activity, Algorithm, Pseudo Code	1. Rig up the circuit as shown in figure 2. place all the required components from multi-sim library 3. click on run button and observe the out put
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	 Narrow Band-Stop Filter.  Circuit Diagram
8	Observation Table, Look-up Table, Output	
9	Sample Calculations	

Copyright ©2017. cAAS. All rights reserved.

10	Graphs, Outputs	  Frequency Response Twin T Active Notch Filter
11	Results & Analysis	The band-pass and band-reject filters are simulated and output is verified
12	Application Areas	Narrow band-pass used in wireless transceiver Band reject filter is used in speaker systems , telephone technology
13	Remarks	
14	Faculty Signature with Date	

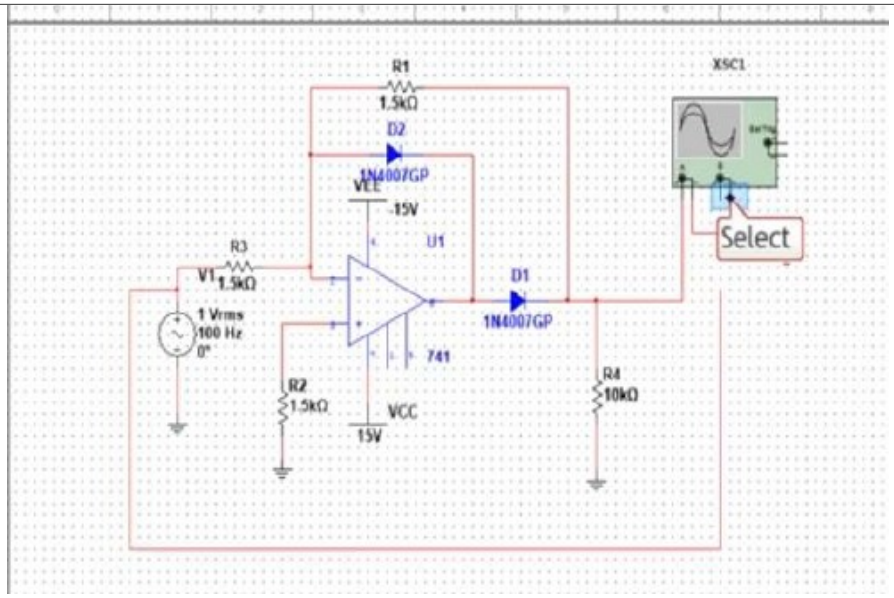
Experiment 11 :PRECISION HALF AND FULL WAVE RECTIFIER

-	**Experiment No.:**	11	**Marks**	10	**Date Planned**		**Date Conducted**	
1	Title	**Precision Half and full wave rectifier**						
2	Course Outcomes	Simulate and analyze analog circuits that uses transistor and ICs for different electronic applications.						
3	Aim	**To simulate and analyze Precision Half and full wave rectifier**						
4	Material / Equipment Required							
5	Theory, Formula,	When forward biased voltage is less than 0.7V, then diode is not conducting. In						

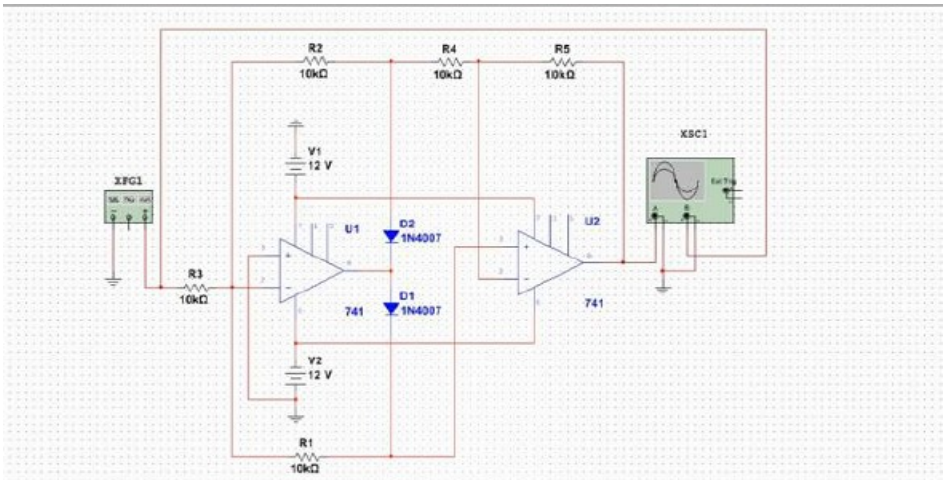
Copyright ©2017. cAAS. All rights reserved.

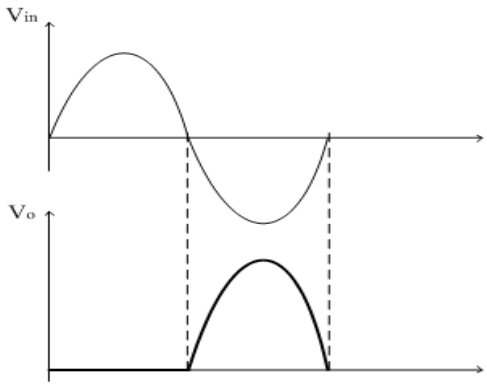
	Principle, Concept	case of normal power rectifier input applied is much larger than 0.7V. So diode is not operated. Therefore Op-amp is used to help diode to conduct. The precision rectifiers are classified in two categories. 1.**Precision Half wave rectifier** 2. **Precision Full wave Rectifier** **1. Precision Half wave rectifier (HWR) :** In HWR, the diode conducts in one of the half cycles of applied ac input signal. Because of this we can classify HWR as positive PHWR (output is positive) and negative PHWR (output is negative). In positive half cycle of applied ac input signal output of op-amp is negative, so diode D1 is forward biased and D2 is reversed biased. The output of op-amp is virtually shorted to ground and output voltage is zero. In negative half cycle of applied ac input signal output of op-amp is positive, so diode D2 is forward biased and D1 is reversed biased. Non-saturated types of precision half wave rectifiers are suitable for high frequency applications. In HWR, the diode conducts in one of the half cycles of applied ac input signal. Design: In positive half cycle of applied ac input signal output of op-amp is negative, so diode D1 is forward biased and D2 is reversed biased. The output of op-amp is virtually shorted to ground and prevented going into saturation. Thus output voltage is zero. ∴Vo=0 V In negative half cycle of applied ac input signal output of op-amp is positive, so diode D2 is forward biased and D1 is reversed biased. The circuit now works as an inverting amplifier with gain of(-Rf/R1) Vo=Vin×A But in negative half cycle input magnitude is negative therefore we get, Vo=(-V_in)[-Rf/R1] ∴Vo=Rf/R1(Vin) Thus in negative half cycle output is positive with a gain of(Rf/R1). **2.Precision Full wave Rectifier:** In PFWR, for both the half cycles output is produced & in one direction only. In positive half cycle of applied ac input signal, output of first op-amp (A1) is Negative. Therefore diode D2 is forward biased & diode D1 is reverse biased.
6	Procedure, Program, Activity, Algorithm, Pseudo Code	
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	Half-wave:

Copyright ©2017. cAAS. All rights reserved.

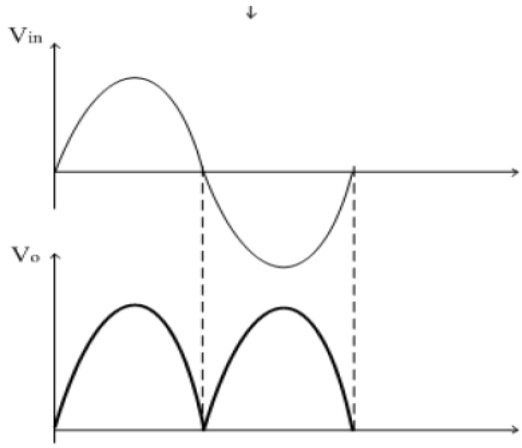


full wave:



8	Observation Table, Look-up Table, Output	
9	Sample Calculations	
10	Graphs, Outputs	Half wave : 

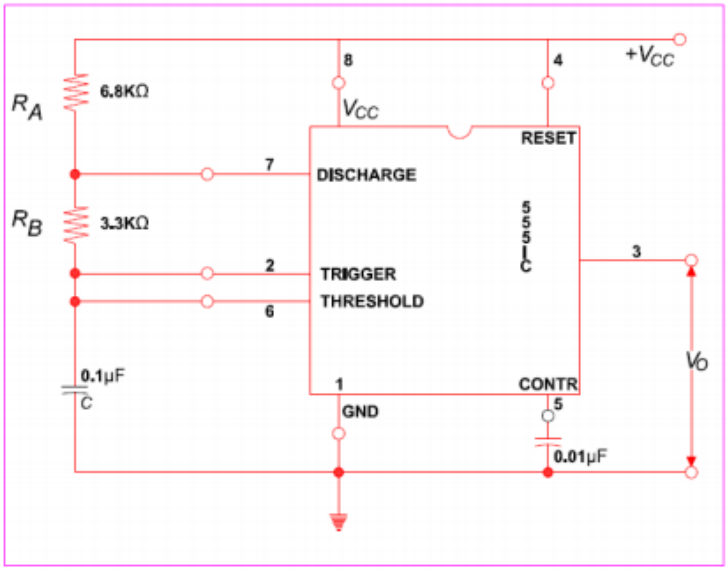
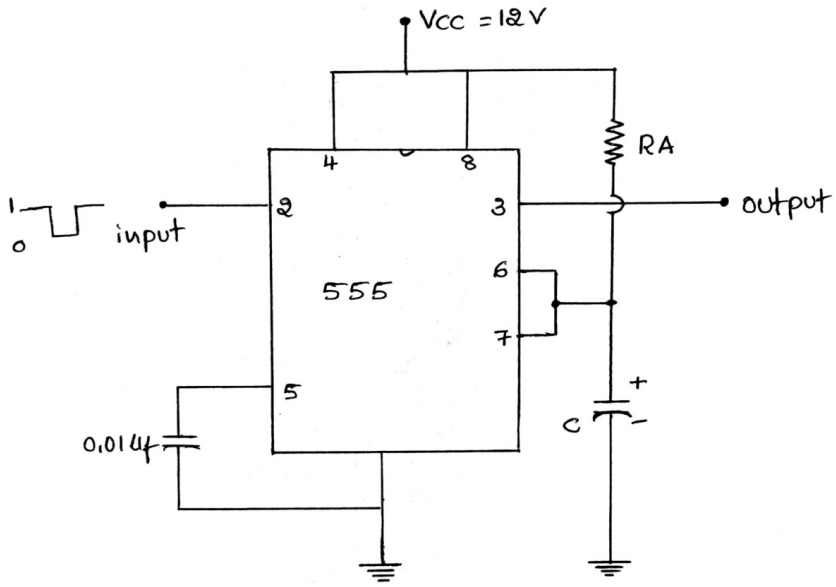
Copyright ©2017. cAAS. All rights reserved.

		full wave: 
11	Results & Analysis	The Precision Half and full wave rectifier simulated and output is verified
12	Application Areas	Used in instrumentation application
13	Remarks	
14	Faculty Signature with Date	

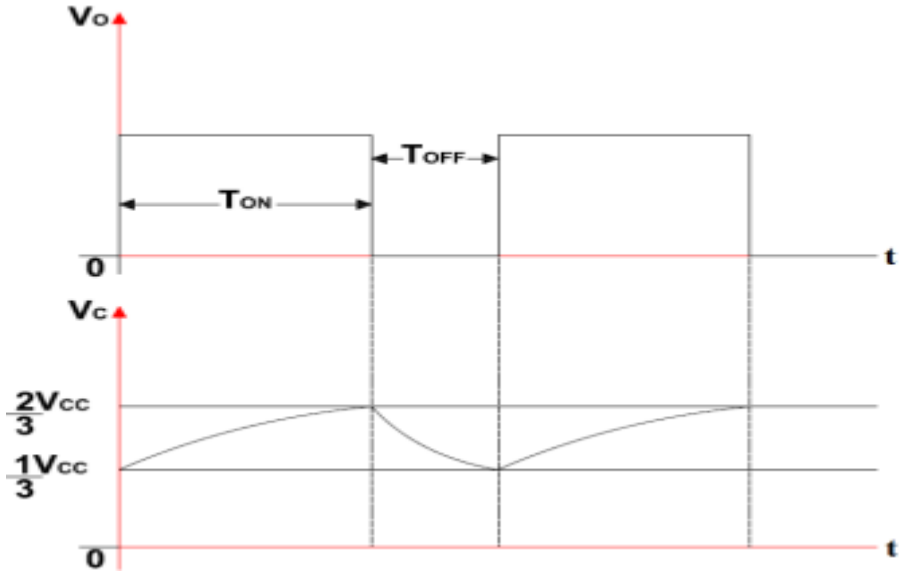
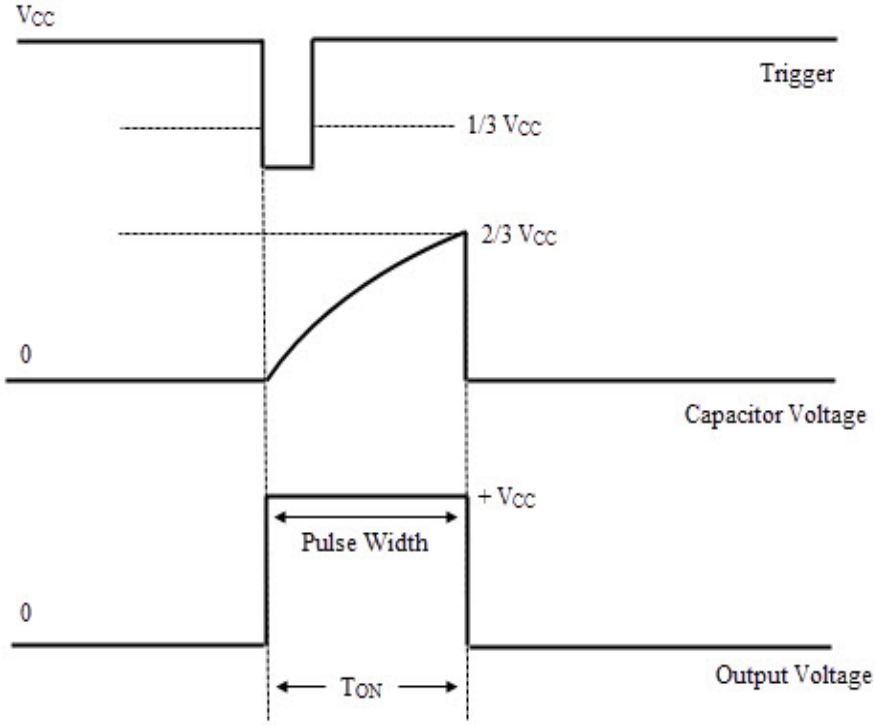
Experiment 12 : Monostable and Astable multivibrator

-	**Experiment No.:**	12	**Marks**	10	**Date Planned**		**Date Conducted**	
1	Title	**Monostable and Astable multivibrator**						
2	Course Outcomes	Simulate and analyze analog circuits that uses transistor and ICs for different electronic applications.						
3	Aim	To simulate and analyze Monostable and Astable multivibrator						
4	Material / Equipment Required							
5	Theory, Formula, Principle, Concept	**Astable multivibrator:** The basic 555 timer based Astable multivibrator circuit is depicted in fig 1. Initially, capacitor C is fully discharged, which forces the output to go to the HIGH state. An open discharge transistor allows capacitor C to charge from +Vcc through resistors R1 and R2. When the voltage across C exceeds +2Vcc /3, the output enters the LOW state and the discharge transistor is switched ON at the same time. Capacitor C starts to discharge through R2 and the discharge transistor inside the IC. When the voltage across C falls below + Vcc /3, the output enters the HIGH state. The charge and discharge cycles repeat and the circuit behaves as a free running multivibrator. Terminal-4 of the IC is the RESET terminal. Usually, it is connected to +Vcc. If the voltage at this terminal is driven below 0.4, the output is forced to the LOW state overriding command pulses at terminal-2 of the IC. HIGH						

Copyright ©2017. cAAS. All rights reserved.

		state and LOW state time periods are governed by the charge (+ Vcc /3 to +2Vcc / 3) and discharge (+2Vcc /3 to +Vcc /3) timings. These are given by (1) and (2) respectively. HIGH state time period, T_{HIGH}= 0.69 x (R1+R2) x C LOW state time period, T_{LOW}= 0.69 x R2 x C
6	Procedure, Program, Activity, Algorithm, Pseudo Code	1. Rig up the circuit as shown in figure 2. place all the required components from multi-sim library 3. click on run button and observe the out put
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	**Astable multivibrator:**  **Fig. 3** Astable multivibrator circuit schematic monostable multi-vibrator: 
8	Observation Table,	

Copyright ©2017. cAAS. All rights reserved.

	Look-up Table, Output	
9	Sample Calculations	
10	Graphs, Outputs	Astable multi-vibrator  monostable multi-vibrator 
11	Results & Analysis	The Astable and manostable multi-vibrator is simulated and output is verified
12	Application Areas	**Astable multivibrator:** 2. Square wave oscillator. 2 Free running ramp generator.

Copyright ©2017. cAAS. All rights reserved.

		Manostable multivibrator: 2. Frequency divider. 2. Pulse stretcher.
13	Remarks	
14	Faculty Signature with Date	