SRI KRISHNA INSTITUTE OF TECHNOLOGY

(Accredited by NAAC, Approved by A.I.C.T.E. New Delhi, Recognised by Govt. of Karnataka & Affiliated to V.T U., Belgaum)

#29, Chimney Hills, Hesaraghatta Main Road, Chikkabanavara Post, Bangalore- 560090

Department of Computer Science and Engineering

Academic Year: 2022-2023	Semester: 3
Course Name: COMPUTER ORGANIZATION AND ARCHITECTURE	Course Code: 21CS34
Total Contact hours: 40	Credits:3
SEE Marks: ; CIE: 50;50	Total Marks: 100
Course Plan Author: Mrs Sowmya C V	Date: 26/09/2022

Course Prerequisites: Basic knowledge of computer, functionalities of the computer components. Basic operations of computer. Central processing unit and operation, Arithmetic Operations with binary representation

Course Objectives:

- Understand the organization and architecture of computer systems, their structure and operation
- Illustrate the concept of machine instructions and programs
- Demonstrate different ways of communicating with I/O devices
- Describe different types memory devices and their functions
- Explain arithmetic and logical operations with different data types
- Demonstrate processing unit with parallel processing and pipeline architecture

Course Outcomes:

CO Number	Course Outcome At the end of the course, student should be able to . . .	Blooms' Level
CO1	Explain the organization and architecture of computer systems with machine instructions and programs	L2
CO2	Analyze the input/output devices communicating with computer system	L3
CO3	Demonstrate the functions of different types of memory devices	L2
CO4	Apply different data types on simple arithmetic and logical unit	L3
CO5	Analyze the functions of basic processing unit, Parallel processing and pipelining	L4

Program Outcomes and Program Specific Outcomes

PO, PSO	1.Engineering Knowledge; 2.Problem Analysis; 3.Design / Development of Solutions; 4.Conduct Investigations of Complex Problems; 5.Modern Tool Usage; 6.The Engineer and Society; 7.Environment and Sustainability; 8.Ethics; 9.Individual and Teamwork; 10.Communication; 11.Project Management and Finance; 12.Life-long Learning; PSO1.:Accomplish The Skills To Design And Develop Computer Applications In Areas Related To Computer And Networking Systems, Artificial Intelligence , Data Processing And Iot Of Varying Complexity PSO2. Dexterity To Apply Modern Computing Languages And Platforms In Creating Career Paths To Be An Entrepreneur And Relish For Higher studies. PSO3: Ability To Use And Enhance Open Ended Programming Environment To Deliver A Quality Product.

CO – PO Mapping

Course Outcomes	Program Outcomes														
	PO1	PO2	PO 3	PO 4	PO 5	PO 6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	2	1	1	-		1						2	3		2
CO2	1		2			1						2	2	1	
CO3	3	1	2									1	2	2	
CO4	2	3	3	2		1						2	2	1	
CO5	2	2	2										1		

Course Content (Syllabus)

Module 1:

Basic Structure of Computers: Basic Operational Concepts, Bus Structures, Performance – Processor Clock, Basic Performance Equation, Clock Rate, Performance Measurement.

Machine Instructions and Programs: Memory Location and Addresses, Memory Operations, Instructions and Instruction Sequencing, Addressing Modes

Textbook 1: Chapter1 – 1.3, 1.4, 1.6 (1.6.1-1.6.4, 1.6.7), Chapter2 – 2.2 to 2.5

RBT: L1, L2

Module 2

Input/Output Organization: Accessing I/O Devices, Interrupts – Interrupt Hardware, Direct Memory Access, Buses, Interface Circuits

Textbook 1: Chapter4 – 4.1, 4.2, 4.4, 4.5, 4.6

RBT: L1, L2

Module 3

Memory System: Basic Concepts, Semiconductor RAM Memories, Read Only Memories, Speed, Size, and Cost, Cache Memories – Mapping Functions, Virtual memories

Textbook 1: Chapter 5 – 5.1 to 5.4, 5.5 (5.5.1, 5.5.2)

RBT: L1, L2

Module 4

Arithmetic: Numbers, Arithmetic Operations and Characters, Addition and Subtraction of Signed Numbers, Design of Fast Adders, Multiplication of Positive Numbers **Basic Processing Unit:** Fundamental Concepts, Execution of a Complete Instruction, Hardwired control, Microprogrammed control

Textbook 1: Chapter2-2.1, Chapter6 – 6.1 to 6.3

Textbook 1: Chapter7 – 7.1, 7.2,7.4, 7.5

RBT: L1, L2

Module 5

Pipeline and Vector Processing: Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction Pipeline, Vector Processing, Array Processors

Textbook 2: Chapter 9 – 9.1, 9.2, 9.3, 9.4, 9.6, 9.7

RBT: L1, L2

Schedule of Instruction

Sl.no	Class no	Module	Topic	Reference (Book, Page no.)	Course Outcome	Delivery mode
1	1	**Module1:**	**Basic Structure of Computers:** Basic Operational Concepts	T1, 2-7	CO1	L
2	2		Bus Structures	T1, 8-9	CO1	L
3	3		Performance – Processor Clock	T1, 13-14	CO1	L/V
4	4		Basic Performance Equation,	T1, 14	CO1	L/V
5	5		Clock Rate, Performance Measurement.	T1, 16-17	CO1	L
6	6		**Machine Instructions and Programs:** Memory Location and Addresses	T1, 33-36	CO1	L
7	7		Memory Operations	T1, 36	CO1	L

8	8		Instructions and Instruction Sequencing	T1, 37-47	CO1	L
9	9		Addressing Modes	T1, 48	CO1	L/V
10	10	**Module - 2**	**Input/Output Organization**	T1, 203	CO2	L
11	11		Introduction to IO operations	T1, 204	CO2	L
12	12		Accessing I/O Devices	T1, 204	CO2	L
13	13		Introduction to Interrupts	T1, 208-209	CO2	L
14	14		Interrupt Hardware	T1, 210	CO2	L
15	15		Direct Memory Access	T1, 234-237	CO2	L
16	16		Buses,	T1, 240-247	CO2	L
17	17		Interface Circuits	T1, 248-257	CO2	L
18	18	**Module 3:**	**Memory System:** Basic Concepts	T1, 292	CO3	L
19	19		Semiconductor RAM Memories	T1, 295-308	CO3	L
20	20		Read Only Memories	T1, 309-311	CO3	L
21	21		Flash memory	T1, 312	CO3	L
22	22		Speed,	T1, 313	CO3	L
23	23		Size, and Cost,	T1, 313	CO3	L/V
24	24		Cache Memories	T1, 314	CO3	L
25	25		Mapping Functions	T1, 316	CO3	L
26	26		Virtual memories	T1, 337	CO3	L
27	27	**Module 4:**	**Arithmetic:** Numbers	T1, 367	CO4	L
28	28		Arithmetic Operations	T1, 368	CO4	L
29	29		Arithmetic and logical Characters	T1, 368	CO4	L/V
30	30		Addition and Subtraction of Signed Numbers	T1, 369	CO4	L
31	31		Design of Fast Adders	T1, 371	CO4	L

32	32		Multiplication of Positive Numbers	T1, 376	CO4	L
33	33		**Basic Processing Unit:** Fundamental Concepts	T1, 412	CO4	L
34	34		Execution of a Complete Instruction	T1, 421	CO4	L
35	35		Hardwired control	T1, 425	CO4	L
36	36		Microprogrammed control	T1, 429	CO4	L
37	37	**Module 5:**	**Pipeline and Vector Processing:** Parallel Processing,	T2, 299	CO5	L
38	38		Pipelining,	T2, 302	CO5	L
39	39		Arithmetic Pipeline	T2, 307	CO5	L
40	40		Instruction Pipeline	T2, 310	CO5	L
41	41		Vector Processing,	T2, 319	CO5	L
42	42		Array Processors	T2, 326	CO5	L
43	43					
44	44					
45	45					
46	46					

**L – Lecture, V- Videos or any other mode*

Textbooks	
T1	Carl Hamacher, Zvonko Vranesic, Safwat Zaky, Computer Organization, 5th Edition, Tata McGraw Hill
T2	M. Morris Mano, Computer System Architecture, PHI, 3rd Edition
T3	
T4	
Reference books	
R1	William Stallings: Computer Organization & Architecture, 9th Edition, Pearson 2008
R2	
R3	
R4	

	Web links and Video Lectures (e-Resources):
1	https://sites.google.com/skit.org.in/psp-website/about-faculty
2	https://nptel.ac.in/courses/106/103/106103068/
3	https://nptel.ac.in/content/storage2/courses/106103068/pdf/coa.pdf
4	https://nptel.ac.in/courses/106/105/106105163/
5	https://nptel.ac.in/courses/106/106/106106092/
6	https://nptel.ac.in/courses/106/106/106106166/
7	http://www.nptelvideos.in/2012/11/computer-organization.html
8	https://www.geeksforgeeks.org/computer-organization-and-architecture-tutorials/

Assessment Schedule:

Sl.No.	Assessment type	Contents	CO	Duration In Hours	Marks	Date & Time
1	**CIE Test 1**	M1 and M2	CO 1, 2	1Hr 15Min	50	
2	**CIE Test 2**	M3 and M4	C0 3,4	1Hr 15Min	50	
	CIE Test 3	M4 nad M5	CO 4,5	1Hr 15Min	50	
3	**Assignment 1**	**M1 and M2**				
4	**Assignment 2**	**M3 and M4**				
5	**Seminar *(or any planned activtiy)***	**Seminar on M5**				
6	**Semester End Examination**					

Seminar: Group of 6-8 students
Module 1,2,3,4 & 5

CIE + SEE = 50 + 50 = 100 marks

Faculty Incharge DAC Chairman

** *Please mention as per the scheme.*