Academic Year: 2021-2022	Semester: III
Course Name: Computer Organization	Course Code: 21CS34
Total Contact hours: 3	Credits:3
SEE Marks:50; CIE:50	Total Marks: 100
Course Plan Author: Ms.Ramya H	Date: 28/09/2022

Course Prerequisites: Basics of Analog and Digital concepts.

Course Objectives:

CLO 1. Understand the organization and architecture of computer systems, their structure and operation

CLO 2. Illustrate the concept of machine instructions and programs

CLO 3. Demonstrate different ways of communicating with I/O devices

CLO 4. Describe different types memory devices and their functions

CLO 5. Explain arithmetic and logical operations with different data types

CLO 6. Demonstrate processing unit with parallel processing and pipeline architecture

Course Outcomes:

At the end of the course the student will be able to:

CO 1. Explain the organization and architecture of computer systems with machine instructions and programs

CO 2. Analyze the input/output devices communicating with computer system

CO 3. Demonstrate the functions of different types of memory devices

CO 4. Apply different data types on simple arithmetic and logical unit

CO 5. Analyze the functions of basic processing unit, Parallel processing and pipelining

CO Number	Course Outcome At the end of the course, student should be able to . . .	Blooms' Level
CO1	Explain the organization and architecture of computer systems with machine instructions and programs	L2
CO2	Analyze the input/output devices communicating with computer system	L3
CO3	Demonstrate the functions of different types of memory devices	L2
CO4	Apply different data types on simple arithmetic and logical unit	L3
CO5	Analyze the functions of basic processing unit, Parallel processing and pipelining	L4

Program Outcomes and Program Specific Outcomes

PO1	Engineering Knowledge;
PO2	Problem Analysis;

PO3	Design / Development of Solutions;
PO4	Conduct Investigations of Complex Problems;
PO5	Modern Tool Usage;
PO6	The Engineer and Society;
PO7	Environment and Sustainability;
PO8	Ethics;
PO9	Individual and Teamwork;
PO10	Communication;
PO11	Project Management and Finance;
PO12	Life-long Learning;
PSO1	Adapt, Contribute Innovate ideas in the field of Artificial Intelligence and Machine Learning
PSO2	Enrich the abilities to qualify for Employment, Higher studies and Research in various domains of Artificial Intelligence and Machine Learning such as Data Science, Computer Vision, Natural Language Processing with ethical values
PSO3	Acquire practical proficiency with niche technologies and open source platforms and become Entrepreneur in the domain of Artificial Intelligence and Machine Learning

CO – PO Mapping

Course Outcomes	Program Outcomes														
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	2	1	1	-		1						2	3		2
CO2	1		2			1						2	2	1	
CO3	3	1	2									1	2	2	
CO4	2	3	3	2		1						2	2	1	
CO5	2	2	2										1		

Course Content (Syllabus)

Module 1	**Contact Hours**

Basic Structure of Computers: Basic Operational Concepts, Bus Structures, Performance – Processor Clock, Basic Performance Equation, Clock Rate, Performance Measurement. Machine Instructions and Programs: Memory Location and Addresses, Memory Operations, Instructions and Instruction Sequencing, Addressing Modes Textbook 1: Chapter1 – 1.3, 1.4, 1.6 (1.6.1-1.6.4, 1.6.7), Chapter2 – 2.2 to 2.5	8
Module 2	
Input/Output Organization: Accessing I/O Devices, Interrupts – Interrupt Hardware, Direct Memory Access, Buses, Interface Circuits Textbook 1: Chapter4 – 4.1, 4.2, 4.4, 4.5, 4.6	8
Module 3	
Memory System: Basic Concepts, Semiconductor RAM Memories, Read Only Memories, Speed, Size, and Cost, Cache Memories – Mapping Functions, Virtual memories Textbook 1: Chapter 5 – 5.1 to 5.4, 5.5 (5.5.1, 5.5.2)	8
Module 4	
Arithmetic: Numbers, Arithmetic Operations and Characters, Addition and Subtraction of Signed Numbers, Design of Fast Adders, Multiplication of Positive Numbers Basic Processing Unit: Fundamental Concepts, Execution of a Complete Instruction, Hardwired control, Microprogrammed control Textbook 1: Chapter2-2.1, Chapter6 – 6.1 to 6.3 Textbook 1: Chapter7 – 7.1, 7.2,7.4, 7.5	8
Module 5	
Pipeline and Vector Processing: Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction Pipeline, Vector Processing, Array Processors Textbook 2: Chapter 9 – 9.1, 9.2, 9.3, 9.4, 9.6, 9.7	8

Schedule of Instruction

Sl.no	Class no	Module	Topic	Reference (Book, Page no.)	Course Outcome	Delivery mode
1	1	**Module1:**	Basic operational concepts, Bus structures	T1, 7-9	CO1	ICT
2	2		Performance- Processor clock	T1,13-14	CO1	ICT
3	3		Basic Performance Equation, Pipelining and Superscalar Operation	T1,14-15	CO1	ICT, Black board
4	4		Clock Rate, Performance	T1,16	CO1	ICT, Black

			Measurement			board
5	5		Memory Location and Addresses, Memory operations	T1,33-36	CO1	ICT, Black board
6	6		Instruction and Instruction Sequencing	T1,36-47	CO1	ICT
7	7		Instruction and Instruction Sequencing	T1,36-47	CO1	ICT
8	8		Addressing Modes	T1,48-56	CO1	ICT, Black board
9	9	**Module 2:**	Accessing I/O devices	204-208	CO2	ICT
10	10		Interrupts- Interrupt Hardware, Enabling and Disabling Interrupts	208-211	CO2	ICT
11	11		Handling multiple devices	213-217	CO2	ICT
12	12		Controlling Device requests, Exception	217-218	CO2	ICT
13	13		Direct Memory Access	234-237	CO2	ICT
14	14		Buses	240-247	CO2	ICT
15	15		Buses	240-247	CO2	ICT
16	16		Interface Circuits-parallel port	248	CO2	ICT
17	17		Interface Circuits- Serial port	257	CO2	ICT
18	18	**Module 3:**	Basic Concepts	292	CO3	ICT
19	19		Semiconductor RAM Memories	295-308	CO3	ICT
20	20		Semiconductor RAM Memories	295-308	CO3	ICT
21	21		Semiconductor RAM Memories	295-308	CO3	ICT
22	22		Read Only Memories	309-312	CO3	ICT
23	23		Speed, Size and Cost	313	CO3	ICT
24	24		Cache Memories	314	CO3	ICT
25	25		Mapping Functions	316	CO3	ICT
26	26		Replacement Algorithms	321	CO3	ICT
27	27		Virtual Memories	337-339	CO3	ICT
28	28	**Module 4:**	Arithmetic Numbers,Arithmetic operations and characters	27	CO4	ICT, Black board
29	29		Addition and Subtraction of signed numbers	368-371	CO4	ICT

30	30		Design of Fast Adders	371-372	CO4	ICT
31	31		Multiplication of Positive Numbers	376	CO4	ICT
32	32		Some Fundamental Concepts of Basic Processing Unit	412-420	CO4	ICT
33	33		Execution of a complete Instruction	421-422	CO4	ICT
34	34		Hard wired Control	425-428	CO4	ICT
35	35		Micro Programmed Control	429-443	CO4	ICT
36	36		Micro Programmed Control	429-443	CO4	ICT
37	37	**Module 5:**	Parallel processing	T2,299	CO5	ICT
38	38		Pipelining	T2,302	CO5	ICT
39	39		Arithmetic pipeline	T2,307	CO5	ICT
40	40		Instruction pipeline	T2310	CO5	ICT
41	41		Vector processing	T2,319-325	CO5	ICT
42	42		Vector processing-Memory Interleaving, supercomputers	T2,319-325	CO5	ICT
43	43		Attached Array Processors	T2326-330	CO5	ICT
44	44		SIMD Array Processors	T2,326-330	CO5	ICT

**L – Lecture, V- Videos or any other mode*

Textbooks	
T1	Carl Hamacher, Zvonko Vranesic, Safwat Zaky, Computer Organization, 5th Edition, Tata McGraw Hill
T2	M. Morris Mano, Computer System Architecture, PHI, 3rd Edition
Reference books	
R1	William Stallings: Computer Organization & Architecture, 9th Edition, Pearson

Web links and Video Lectures (e-Resources):	
1	
2	https://nptel.ac.in/content/storage2/courses/106103068/pdf/coa.pdf
3	https://nptel.ac.in/courses/106/105/106105163/
4	https://nptel.ac.in/courses/106/106/106106092/
5	https://nptel.ac.in/courses/106/106/106106166/
6	https://nptel.ac.in/courses/106/103/106103068/
7	http://www.nptelvideos.in/2012/11/computer-organization.html

Assessment Schedule:						
Sl.No.	**Assessment type**	**Contents**	**CO**	**Duration In Hours**	**Marks**	**Date & Time**
1	**CIE Test 1**	Module 1,2	CO1,CO2	1:00	20	
2	**CIE Test 2**	Module 3,4	CO3,CO4	1:00	20	
	CIE Test 3	Module 5	CO5	1:00	20	
3	**Assignment 1**	Module 1,2	CO1,CO2		10	
4	**Assignment 2**	Module 3,4	CO3,CO4		10	
5	**Seminar *(or any planned activtiy)***	Module 5	CO5		20	

Seminar: Group of 6-8 students
Module 1,2,3,4 & 5

****The sum of total marks of three tests, two assignments, and seminar will be out of 100 marks and will be scaled down to 50 marks.**

CIE + SEE = 50 + 50 = 100 marks

Faculty Incharge DAC Chairman

*** Please mention as per the scheme.*