SRI RAGHAVENDRA EDUCATIONAL INSTITUTIONS SOCIETY®

SRI KRISHNA INSTITUTE OF TECHNOLOGY

(Approved by A.I.C.T.E. New Delhi, Recognized by Govt. of Karnataka, NAAC Accredited & Affiliated to V.T.U Belgaum)

Campus: No. 29, Chimney Hills, Hesaraghatta Main Road, Chikkabanavara Post, Bangalore- 560090

Tel: 080-23721315, 28392221; FAX: 080-23721477

E-mail: principal@skirt.org.in, www.skit.org.in

Department of Artificial Intelligence and Machine Learning

Academic Year: 2022-2023	Semester: III
Course Name: Analog and Digital Electronics	Course Code: 21CS33
Total Contact hours: 40T + 20P	Credits:4
SEE Marks: 50; CIE:50	Total Marks: 100
Course Plan Author: Mrs. G Soujanya	Date: 11-10-2022

Course Prerequisites: Electronics

Course Objectives:

- Explain the use of photo electronics devices, 555 timer IC, Regulator ICs and uA741
- Make use of simplifying techniques in the design of combinational circuits.
- Illustrate combinational and sequential digital circuits
- Demonstrate the use of flipflops and apply for registers
- Design and test counters, Analog-to-Digital and Digital-to-Analog conversion techniques.

CO Number	Course Outcome At the end of the course, student should be able to . . .	Blooms' Level
CO1	Design and analyze application of analog circuits using timer IC, regulated, power supply, op-amp and also explain the basic principles of A/D converter and D/A conversion circuits and develop the same	L3
CO2	Simplify digital circuits using Karnaugh map and Quine-McClusky Method	L3
CO3	Combinational circuits designs simulation using gates	L3
CO4	Design of sequential circuits using flip flops and develop simple HDL programs	L3
CO5	Designing of different data processing circuits, registers and counters and compare same (using gates and flip flops)	L3

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Program Outcomes and Program Specific Outcomes

Program Outcomes	
1.	**Engineering Knowledge:** Apply knowledge of mathematics, science, engineering fundamentals and an engineering specialization to the solution of complex engineering problems.
2.	**Problem Analysis: Identify,** formulate, research literature and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences and engineering sciences
3.	**Design/ Development of Solutions**: Design solutions for complex engineering problems and design system components or processes that meet specified needs with appropriate consideration for public health and safety, cultural, societaland environmental considerations.
4.	**Conduct investigations of complex problems** using research-based knowledge and research methods including design of experiments, analysis and interpretation of data and synthesis of information to provide valid conclusions.
5.	**Modern Tool Usage**: Create, select and apply appropriate techniques, resources and modern engineering and IT tools including prediction and modeling toComplex engineering activities with an under- standing of the limitations.
6.	**The Engineer and Society**: Apply reasoning informed by contextual knowledge to assess societal, health, safety, legal and cultural issues and theConsequent responsibilities relevant to professional engineering practice.
7.	**Environment and Sustainability**: Understand the impact of professional Engineering solutions in societal and environmental contexts and demonstrate knowledge of and need for sustainable development.
8.	**Ethics**: Apply ethical principles and commit to professional ethics and Responsibilities and norms of engineering practice.
9.	**Individual and Team Work**: Function effectively as an individual, and as a member or leader in diverse teams and in multi-disciplinary settings.
10.	**Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as being able to comprehend and write effective reports and design documentation, make effective presentations and give and receive clear instructions.
11.	**Life-long Learning**: Recognize the need for and have the preparation and ability to engage in independent and life- long learning in the broadest contextof technological change.
12.	**Project Management and Finance**: Demonstrate knowledge and understanding of engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multi-disciplinary environments.

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Program Specific Outcomes	
13.	**PSO1**: Adapt, Contribute Innovate ideas in the field of Artificial Intelligence and Machine Learning
14.	**PSO2:** Enrich the abilities to qualify for Employment, Higher studies and Research in various domains of Artificial Intelligence and Machine Learning such as Data Science, Computer Vision, Natural Language Processing with ethical values
15.	**PSO3**: Acquire practical proficiency with niche technologies and open source platforms and become Entrepreneur in the domain of Artificial Intelligence and Machine Learning

CO – PO Mapping

Course Outcomes	**Program Outcomes**														
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	1	2	0	0	0	0	0	0	1	0	2	3	3	2
CO2	2	2	1	0	0	0	0	0	0	0	0	0	0	1	0
CO3	2	0	3	0	2	2	0	0	0	0	0	0	2	0	0
CO4	2	0	2	0	3	2	0	0	0	0	0	0	0	0	0
CO5	3	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Department of Artificial Intelligence and Machine Learning

Course Content (Syllabus)

Module1: BJT Biasing: Fixed bias, Collector to base Bias, voltage divider bias Operational Amplifier Application Circuits: Peak Detector, Schmitt trigger, Active Filters, Non-Linear Amplifier, Relaxation Oscillator, Current-to-Voltage and Voltage-to-Current Converter, Regulated Power Supply Parameters, adjustable voltage regulator, D to A and A to D converter.
Textbook 1: Part A: Chapter 4 (Sections 4.2, 4.3, 4.4), Chapter 7 (Sections 7.4, 7.6 to 7.11), Chapter8 (Sections 8.1 and 8.5), Chapter 9.

Laboratory Component:
1. Simulate BJT CE voltage divider biased voltage amplifier using any suitable circuit simulator.
2. Using ua 741 Opamp, design a 1 kHz Relaxation Oscillator with 50% duty cycle
3. Design an astable multivibrator circuit for three cases of duty cycle (50%, <50% and >50%) using NE 555 timer IC.
4. Using ua 741 opamap, design a window comparator for any given UTP and LTP.

Module2: Karnaugh maps: minimum forms of switching functions, two and three variable Karnaugh maps, four variable Karnaugh maps, determination of minimum expressions using essential prime implicants, Quine-McClusky Method: determination of prime implicants, the prime implicant chart, Petricks method, simplification of incompletely specified functions, simplification using map-entered variables
Textbook 1: Part B: Chapter 5 (Sections 5.1 to 5.4) Chapter 6 (Sections 6.1 to 6.5)

Laboratory Component:
1. Given a 4-variable logic expression, simplify it using appropriate technique and inplement the same using basic gates.

Module3: Combinational circuit design and simulation using gates: Review of Combinational circuit design, design of circuits with limited Gate Fan-in, Gate delays and Timing diagrams, Hazards in combinational Logic, simulation and testing of logic circuits Multiplexers, Decoders and Programmable Logic Devices: Multiplexers, three state buffers, decoders and encoders, Programmable Logic devices.
Textbook 1: Part B: Chapter 8, Chapter 9 (Sections 9.1 to 9.6)

Laboratory Component:
1. Given a 4-variable logic expression, simplify it using appropriate technique and realize the simplified logic expression using 8:1 multiplexer IC.
2. Design and implement code converter I) Binary to Gray (II) Gray to Binary Code

Module4: Introduction to VHDL: VHDL description of combinational circuits, VHDL Models for multiplexers, VHDL Modules. Latches and Flip-Flops: Set Reset Latch, Gated Latches, Edge-Triggered D Flip Flop 3, SR Flip Flop, J K Flip Flop, T Flip Flop.
Textbook 1: Part B: Chapter 10(Sections 10.1 to 10.3), Chapter 11 (Sections 11.1 to 11.7)

Laboratory Component:
1. Given a 4-variable logic expression, simplify it using appropriate technique and simulate the same in HDL simulator
2. Realize a J-K Master / Slave Flip-Flop using NAND gates and verify its truth table. And implement the same in HDL.

Module5: Registers and Counters: Registers and Register Transfers, Parallel Adder with accumulator, shift registers, design of Binary counters, counters for other sequences, counter design using SR and J K Flip Flops.
Textbook 1: Part B: Chapter 12 (Sections 12.1 to 12.5)

Laboratory Component:
1. Design and implement a mod-n (n<8) synchronous up counter using J-K Flip-Flop ICs and demonstrate its working.
2. Design and implement an asynchronous counter using decade counter IC to count up from 0 to n (n<=9) and demonstrate on 7-segment display (using IC-7447)

Department of Artificial Intelligence and Machine Learning

Schedule of Instruction

Sl. no	Class no	Module	Topic	Reference (Book, Page no.)	Course Outcome	Delivery mode
1	2	**Module 2:** Karnaugh maps, Quine-McClusky Method	Minimum forms of switching functions	T1,422	CO2	PPT, Black Board
2	3		Two and three variable Karnaugh maps,	T1,424	CO2	PPT, Black Board
3	4		Four variable Karnaugh maps	T1, 429	CO2	PPT, Black Board
4	5		Determination of minimum expressions using essential prime implicants	T1,429	CO2	PPT, Black Board
5	6		Quine- McClusky Method: determination of prime implicants	T1,454	CO2	PPT, Black Board
6	7		The Prime Implicant Chart	T1,457	CO2	PPT, Black Board
7	8		Petricks method	T1, 460	CO2	PPT, Black Board
8	9		Simplification of incompletely, Specified functions, Simplification using map-entered variables	T1,462, 463	CO2	PPT, Black Board
9	10	**Module 3:** Combinational circuit design using, multiplexers, decoders and programmable	Review of Combinational circuit design, Design of circuits with limited Gate Fan-in, Gate delays and Timing diagrams	T1,504,505, 507	CO3	PPT, Black Board
10	11		Hazards in combinational Logic	T1,509	CO3	PPT, Black Board
11	12		Simulation and testing of logic circuits	T1,515	CO3	PPT, Black Board
12	13		Multiplexers	T1,530	CO3	PPT, Black Board
13	14		Tree state Buffer	T1,536	CO3	PPT, Black Board

14	15		Decoders and Encoders	T1,539	CO3	PPT, Black Board
15	16		Read only memories	T1,541	CO3	PPT, Black Board
16	17		Programmable logic devices	T1,546	CO3	PPT, Black Board
17	18	**Module 4:** Introduction to VHDL	VHDL description of combinational circuits	T1,563	CO4	PPT, Black Board
18	19		VHDL Models for multiplexers	T1,567	CO4	PPT, Black Board
19	20		VHDL Modules	T1,569	CO4	PPT, Black Board
20	21		Latches and Flip-Flops: Set Reset Latch	T1,599	CO4	PPT, Black Board
21	22		Gated Latches	T1,604	CO4	PPT, Black Board
22	23		Edge-Triggered D Flip Flop	T1,608	CO4	PPT, Black Board
23	24		SR Flip Flop, J K Flip Flop	T1,611,613	CO4	PPT, Black Board
24	25		T Flip-Flop	T1,614	CO4	PPT, Black Board
25	26	**Module 5:** Registers and Counters	Registers and Register Transfers	T1,636	CO5	PPT, Black Board
27	28		Registers and Register Transfers	T1,636	CO5	PPT, Black Board
28	29		Shift registers	T1,640	CO5	PPT, Black Board
29	30		Design of binary counters	T1,645	CO5	PPT, Black Board
30	31		Design of binary counter (up counter)	T1,649	CO5	PPT, Black Board
31	32		Counters for other sequences	T1,651	CO5	PPT, Black Board
32	33		Counters for other sequences	T1,651	CO5	PPT, Black Board
33	34		Counter design Using S-R and J-K Flip-Flops	T1,657	CO5	PPT, Black Board

34	35	**Module1:** BJT Biasing, Operational Amplifier Circuits	BJT Biasing: Fixed bias, Collector to base Bias,	T1, 99	CO1	PPT, Black Board
35	36		voltage divider bias Operational Amplifier Application Circuits: peack detector	T1,103,230	CO1	PPT, Black Board
36	37		Schmitt Trigger	T1,235	CO1	PPT Black Board
37	38		Active Filters	T1,248	CO1	PPT, Black Board
38	39		Non-Linear Amplifier, Relaxation Oscillator,	T1,278,279	CO1	PPT, Black Board
39	40		Current-to-Voltage and Voltage-to-Current Converter	T1,282,284	CO1	PPT, Black Board
40	41		Regulated Power Supply Parameters, adjustable voltage regulator	T1,288,298	CO1	PPT, Black Board
41	42		D to A converter, A to D converter.	T1,304,310	CO1	PPT, Black Board

**L – Lecture, V- Videos or any other mode*

Expt. no	**Experiments Name**	**Course Outcome**	**Delivery mode**
1	Simulate BJT CE voltage divider biased voltage amp using any suitable circuit simulator	CO1	Demonstration
2	Using ua 741 Opamp, design a 1 kHz Relaxation Oscillator with 50% duty cycle	CO1	Demonstration
3	Design an astable multivibrator circuit for three cases of duty cycle (50%, <50% and >50%) using NE 555 timer IC.	CO1	Demonstration
4	Using ua 741 opamap, design a window comparator for any given UTP and LTP.	CO1	Demonstration
5	Given a 4-variable logic expression, simplify it using appropriate technique and implement the same using basic gates	CO2	Demonstration
6	Given a 4-variablelogic expression, simplify it using appropriate technique and realize the simplified logic expression using 8:1 multiplexer IC.	CO3	Demonstration

7	Design and implement Code converter 1) Binary to Gray 2) Gray to Binary	CO3	Demonstration
8	Given a 4-variable logic expression, simplify it using appropriate technique and simulate the same in HDL simulator	CO4	Demonstration
9	Realize a J-K Master / Slave Flip-Flop using NAND gates and verify its truth table. And implement the same in HDL.	CO4	Demonstration
10	Design and implement a mod-n (n<8) synchronous up counter using J-K Flip-Flop ICs and demonstrate its working.	CO5	Demonstration
11	Design and implement an asynchronous counter using decade counter IC to count up from 0 to n(n<=9) and demonstrate on 7-segment display (using IC-7447)	CO5	Demonstration

Textbooks	
T1	Charles H Roth and Larry L Kinney, Analog and Digital Electronics, Cengage Learning,2019
Reference books	
R1	Anil K Maini, Varsha Agarwal, Electronic Devices and Circuits, Wiley, 2012.
R2	Donald P Leach, Albert Paul Malvino & Goutam Saha, Digital Principles and Applications, 8th Edition, Tata McGraw Hill, 2015
R3	M. Morris Mani, Digital Design, 4th Edition, Pearson Prentice Hall, 2008.
R4	David A. Bell, Electronic Devices and Circuits, 5th Edition, Oxford University Press, 2008

	Web links and Video Lectures (e-Resources):
1	https://sites.google.com/skit.org.in/21cs33-ade/home
2	Analog Electronic Circuits: https://nptel.ac.in/courses/108/102/108102112/
3	Digital Electronic Circuits: https://nptel.ac.in/courses/108/105/108105132/
4	Analog Electronics Lab: http://vlabs.iitkgp.ac.in/be/
5	Digital Electronics Lab: http://vlabs.iitkgp.ac.in/dec

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Assessment Schedule:

Sl.No.	Assessment type	Contents	CO	Duration In Hours	Marks	Date & Time
1	CIE Test 1	M2, M3	CO2, CO3	1	20	6-12-2022
2	CIE Test 2	M4, M5	CO4, CO5	1	20	6-01-2023
3	CIE Test 3	M1	CO1	1	20	
4	Assignment 1	M2, M3	CO2, CO3		10	
5	Assignment 2	M4, M5	CO4, CO5		10	
6	Lab assessment Marks	M1, M2, M3, M4, M5	CO1-CO5		20	
7	Semester End Examination	M1, M2, M3, M4, M5	CO1-CO5	3	50	

Faculty Incharge DAC Chairman